MILESTONE 1

SKEE2263

Individual

(5% final grade)

OBJECTIVES:

- Familiarization with Altera Quartus for entering, compiling and simulating a logic design.
- Describing a complex digital system using hierarchy, modularity and regularity
- Using the Internet to find solutions of circuit designs.

PART 1: HALF ADDER

Step 1.

Use Quartus schematic entry to input the half adder design.

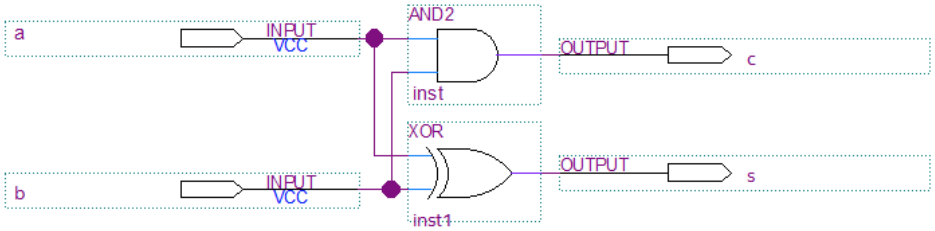

Fig. 1

Step 2.

Compile the design.

If there are no errors, print compilation report as PDF.

Step 3.

Simulate by giving all 4 input combinations for a and b : 00, 01, 10 and 11. Maintain each input combination for 100ns. That means the End Time for the simulation should be 400ns. Check the result with the expected output. When the circuit is error-free, proceed to Step 4.

Step 4.

Convert the module into symbol file. Call it **ha.bsf**.

Step 5.

Print the following 3 pages as PDF. You must choose landscape orientation.

Page 1: Schematic of half adder: Printscreen then convert to PDF.

Page 2: Compilation report

Page 3: Annotated simulation output waveform: **This is not the same as the simulation input.** Printscreen first, then in MSPaint or similar software, highlight the important information. Save as PDF.

PART 2: FULL ADDER

Step 1.

Use Quartus schematic entry to input two instances of half adder symbols from Part 1 Step 4. Combine the two half adders with an **or2** gate to build a full adder.

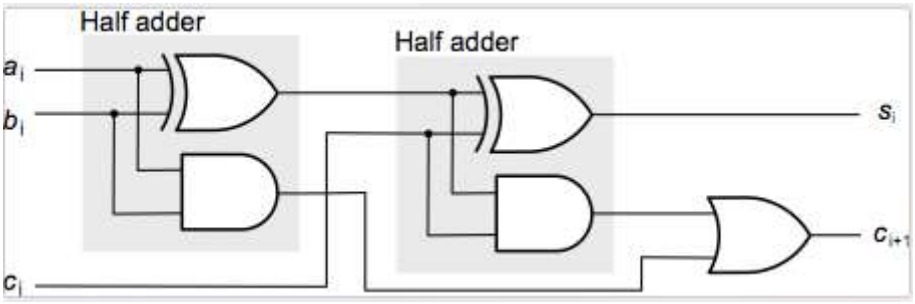

Fig 2.

Step 2.

Compile the design.

If there are no errors, print compilation report as PDF.

Step 3:

Simulate using all 8 input combinations 000 through 111. Maintain each input combination for 100ns. That means the End Time for the simulation should be 800ns. Check the result with the expected output. When the circuit is error-free, proceed to Step 4.

Step 4.

Convert the module into symbol file. Call it **fa.bsf**.

Step 5.

Print the following 3 pages as PDF. You must choose landscape orientation.

Page 4: Schematic of full adder..

Page 5: Compilation report

Page 6: Annotated simulation output waveform..

PART 3: RIPPLE CARRY ADDER

Step 1.

Use Quartus schematic entry to input four instances of full adder symbols from Part 2 Step 4. Combine to build the ripple carry as follows.

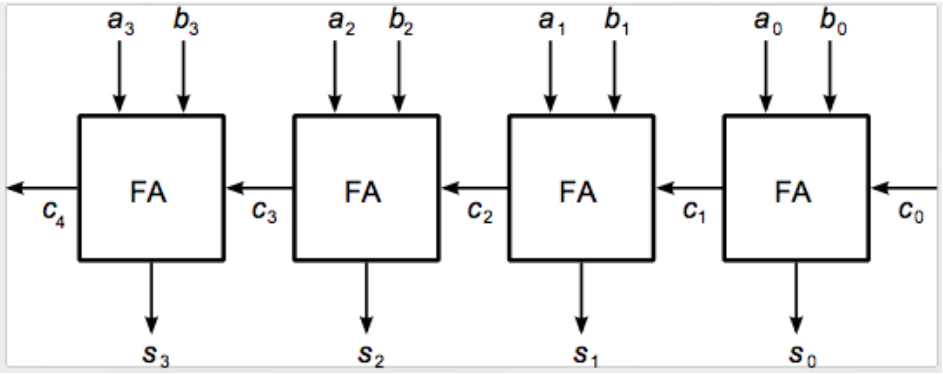

Fig 3.

Step 2.

Compile the design.

If there are no errors, print compilation report as PDF.

Step 3:

In the Table below, fill in columns COUT and S[3:0] so you know what is the expected output for each input combination. Columns A, B and S are in hex.

Table 1A3

A[3:0]	B[3:0]	CIN	COUT	S[3:0]	Comply?
0	0	0			
F	F	1			
F	0	0			
0	F	0			
F	0	1			
0	F	1			
8	8	0			
A	5	0			
C	3	0			
3	C	1			

In the simulation waveform input, use bus groups for A, B and S signal. (A bunch of related signals are called a bus.) Use hexadecimal system.

Simulate using the given test data. Then mark with the adder complies with the expected results. Simulate using the 10 input combinations given below. Maintain each input combination for 100ns. That means the End Time for the simulation should be 1000ns. When the circuit is error-free, proceed to Step 4.

Step 4.

Print the following 4 pages as PDF. You must choose landscape orientation.

Page 7: Schematic of ripple carry adder..

Page 8: Compilation report

Page 9: Annotated simulation output waveform..

Page 10: References. On this page, list all web sites, articles or books you referred in completing the assignment. You must any citation format but be consistent.

Step 5.

Combine all 10 PDF pages into 1 PDF document. Add the plagiarism declaration below as the front cover. Upload to elearning.utm.my.

PLAGIARISM DECLARATION

1. I know that plagiarism means taking and using the ideas, writings, works or inventions of another as if they were one's own. I know that plagiarism not only includes verbatim copying, but also the extensive use of another person's ideas without proper acknowledgement (which includes the proper use of quotation marks). I know that plagiarism covers this sort of use of material found in textual sources and from the Internet.
2. I acknowledge and understand that plagiarism is wrong.
3. I understand that my research must be accurately referenced. I have followed the rules and conventions concerning referencing and citation.
4. I declare that all material in this assignment is my own work and does not involve plagiarism.
5. I have not allowed, nor will I in the future allow, anyone to copy my work with the intention of passing it off as their own work.

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