

Chapter 4

Logic Gates

SKEE1223 Digital Electronics

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Overview

- 1 Basic Gates
- 2 Logic Circuits
- 3 Other Logic Gates
- 4 Digital Integrated Circuits

Logic Gates Overview

Logic gates:

- Primitive / fundamental building blocks for all digital circuits
- At least one input
- Only one output
- Output depends on the function of the gate and the combination of all its inputs

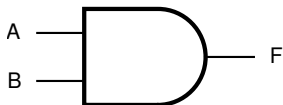


Describing Gates

- Graphical symbol
 - Distinctive or rectangular shape
 - Used in circuit diagrams
- Boolean Algebra:
 - Mathematical method
- Truth table:
 - Canonical truth table contains all input combinations
 - Each row show input-output relationship
- Timing diagram
 - Shows the input-output behavior graphically

AND Gate

- High output only if **all** inputs are high



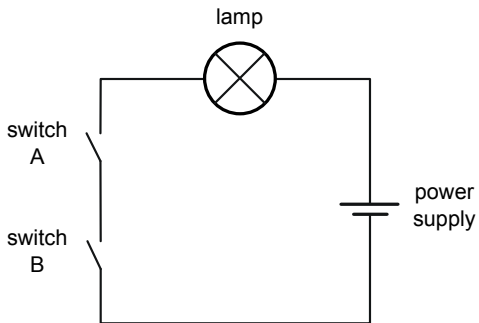
Input		Output
A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

- Described by Boolean expression:

$$F = AB$$

- Can also use $F = A \cdot B$, $F = A \& B$, $F = A \wedge B$

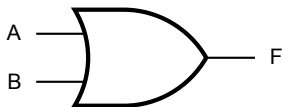
Switch Representation of AND Gate



A	B	lamp
OPEN	OPEN	OFF
OPEN	CLOSED	OFF
CLOSED	OPEN	OFF
CLOSED	CLOSED	ON

OR Gate

- High output if **any** input is high



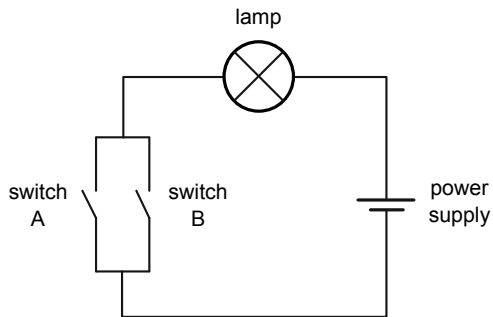
Input		Output
A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

- Described by Boolean expression:

$$F = A + B$$

- Can also use $F = A|B$, $F = A \vee B$

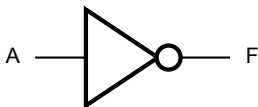
Switch Representation of OR Gate



A	B	lamp
OPEN	OPEN	OFF
OPEN	CLOSED	ON
CLOSED	OPEN	ON
CLOSED	CLOSED	ON

NOT Gate

- Inverts its input
- NOT gate is also known as inverter



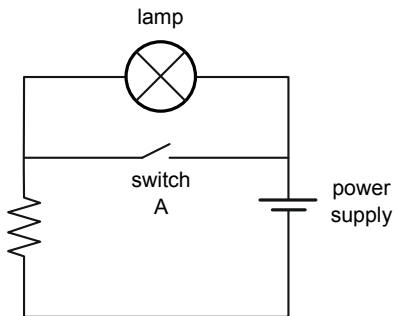
Input	Output
A	F
0	1
1	0

- Described by Boolean expression:

$$F = \bar{A}$$

- Can also use $F = A'$, $F = \sim A$

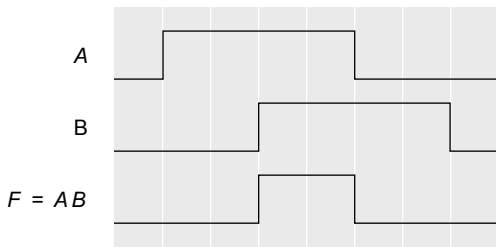
Switch Representation of NOT Gate



A	lamp
OPEN	ON
CLOSED	OFF

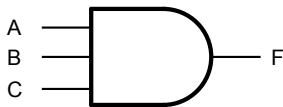
Timing Diagrams

- Shows the relationship between inputs and outputs



Gates with More than 2 Inputs

- AND gates: output is true when **all inputs are true**

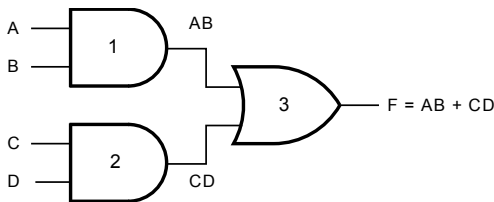


Input			Output
A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

- OR gates: output is true when **any inputs is true**
- NOT gates: cannot have more than 1 input

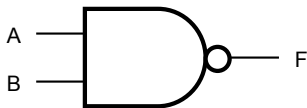
Gates with More than 2 Inputs

- Gates can be connected to make a **logic network**
- Output can be connected to 1 or more inputs
- Input can be connected to only 1 output
- Most common is AND-OR network
- Network $F = AB + CD$ is shown



NAND Gate

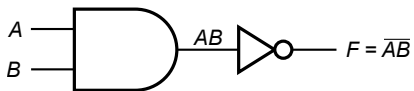
Output is low when all inputs are high, and high otherwise.



Input		Output
A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

$$\begin{aligned} F &= \overline{A \cdot B} \\ &= (AB)' \end{aligned}$$

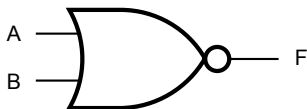
NAND Gate Equivalent Circuit



$$\begin{aligned} F &= \overline{A \cdot B} \\ &= (AB)' \end{aligned}$$

NOR Gate

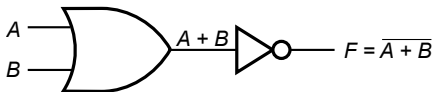
Output is high where all inputs are low, and low otherwise



Input		Output
A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

$$\begin{aligned} F &= \overline{A+B} \\ &= (A+B)' \end{aligned}$$

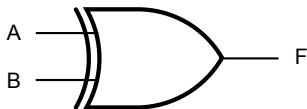
NOR Gate Equivalent Circuit



$$\begin{aligned} F &= \overline{A + B} \\ &= (A + B)' \end{aligned}$$

XOR Gate

Output is high if one and only one input is high.

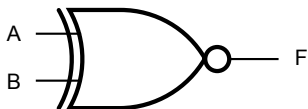


Input		Output
A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

$$\begin{aligned}F &= A \oplus B \\ &= \bar{A}B + A\bar{B}\end{aligned}$$

XNOR Gate

Output is high when both inputs are equal.

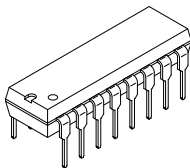


Input		Output
A	B	F
0	0	1
0	1	0
1	0	0
1	1	1

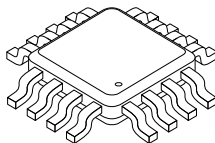
$$\begin{aligned}F &= A \odot B \\ &= \bar{A} \cdot \bar{B} + A \cdot B \\ &= (A \equiv B)\end{aligned}$$

Overview of Digital ICs

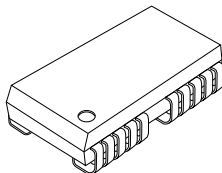
- Collection of gates on a single chip of silicon



DIP.

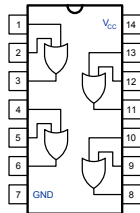
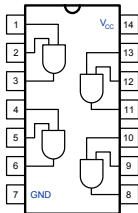
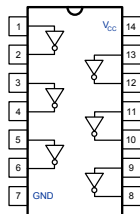
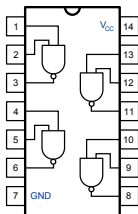
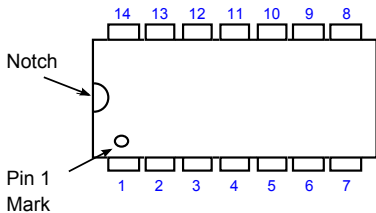


SOIC.

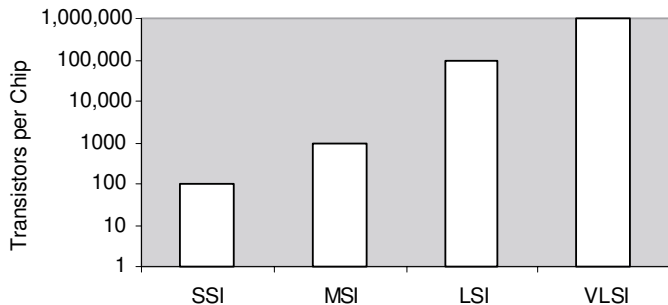


PLCC.

14-pin DIP integrated circuits

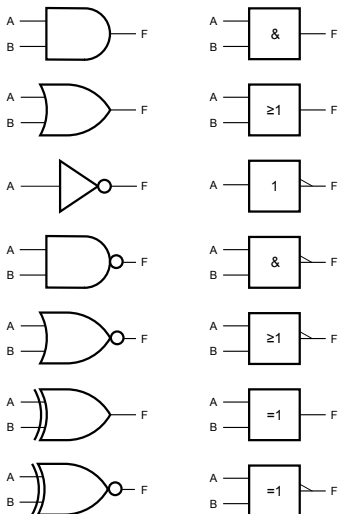


Relative Chip Sizes



Complexity	Acronym	Number of gates	Example
Small scale integration	SSI	≤ 10	Individual gates
Medium scale integration	MSI	10 – 100	Flip-flops, registers
Large scale integration	LSI	100 – 1,000	Memories
Very large scale integration	VLSI	$\geq 1,000$	Microprocessors

ANSI vs IEEE Logic Symbols



Summary of Gate Functions

Gate	Description
NOT	Inverts the input (HIGH becomes LOW, LOW becomes HIGH)
AND	Outputs HIGH if all the inputs are HIGH; otherwise, outputs LOW
OR	Outputs HIGH if at least one of the inputs is HIGH; otherwise, outputs LOW
NAND	Outputs HIGH if all the inputs are LOW; otherwise, outputs LOW
NOR	Outputs HIGH if at least one of the inputs is LOW; otherwise, outputs LOW
XOR	Outputs HIGH if one, and only one, of the inputs is HIGH; otherwise, outputs LOW
XNOR	Outputs HIGH if one, and only one, of the inputs is LOW; otherwise, outputs LOW



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