

Chapter 7

Combinational Logic Networks

SKEE1223 Digital Electronics

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Overview

- 1 Overview
- 2 Design Example 1
- 3 Design Example 2
- 4 Universal Gates
- 5 NAND-NAND Networks

Design Process

Conceptualize	Get “the big picture” or overall view. During this step, determine the number of inputs and outputs from the specifications.
Truth Table	Obtain the truth table for the outputs based on their relationship to the input.
Equations	Simplify the Boolean expression for each output. Use Karnaugh maps or Boolean algebra.
Schematic	Draw the circuit diagram that represents the simplified Boolean expressions. Verify the design by analyzing or simulating the circuits.

Design Example 1

Majority decider circuit

Problem:

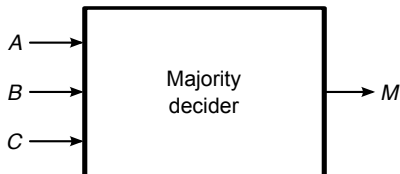
Implement a three-input majority decider circuit.

1 Understand the Specification

A majority decider circuit outputs a 1 if the majority of its inputs are 1. For a 3-input circuit, the output is 1 if 2 or 3 inputs are 1.

■ Optional

Sketch a top-level block diagram showing all inputs and outputs. Label all inputs and outputs.



Design Example

Majority decider circuit

2 Truth Table

Carefully fill in the truth table.

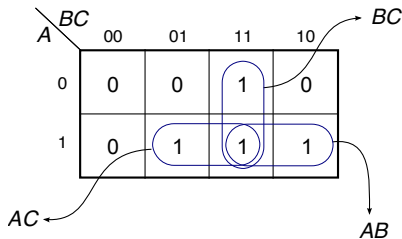
A	B	C	M
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Design Example

Majority decider circuit

3 Equations

Get the equations using K-map (recommended) or Boolean algebra.

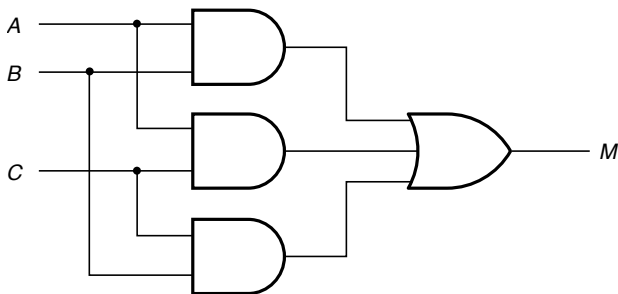


Design Example

Majority decider circuit

4 Circuit Diagram

Finally, draw the circuit schematic.



Design Example 2

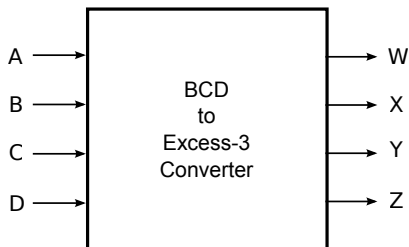
BCD to XS3 Converter

Problem:

Implement a BCD to Excess-3 converter circuit.

1 Understand the Specification

BCD and XS3 codes are 4-bit codes. We can assign ABCD to input and WXYZ to output.



Design Example

BCD to XS3 Converter

2 Truth Table

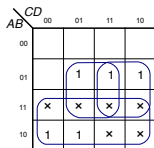
Carefully fill in the truth table. Inputs 1010 - 1111 are don't cares.

Input				Output			
A	B	C	D	W	X	Y	Z
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0
1	0	1	0	x	x	x	x
1	0	1	1	x	x	x	x
1	1	0	0	x	x	x	x
1	1	0	1	x	x	x	x
1	1	1	0	x	x	x	x
1	1	1	1	x	x	x	x

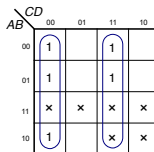
Design Example

BCD to XS3 Converter

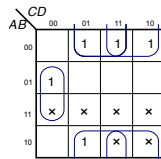
3 Equations



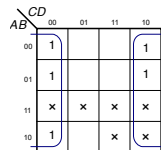
$$W = A + BC + BD$$



$$Y = CD + \bar{C}\bar{D}$$



$$X = \bar{B}C + \bar{B}D + B\bar{C}\bar{D}$$

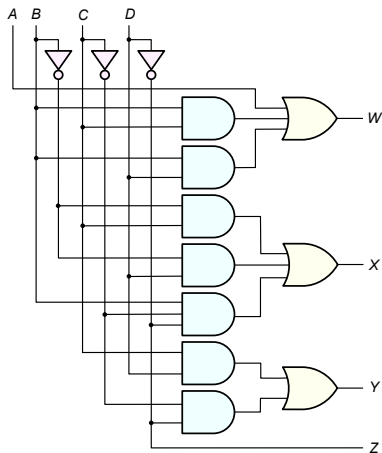


$$Z = \bar{D}$$

Design Example

BCD to XS3 Converter

4 Schematic Diagram



Review of DeMorgan's Theorem

$$\overline{AB} = \bar{A} + \bar{B}$$

$$\overline{A + B} = \bar{A}\bar{B}$$

and

$$AB = \overline{\bar{A} + \bar{B}}$$

$$A + B = \overline{\bar{A}\bar{B}}$$

DeMorgan's Theorem Applied to NAND Gates

A	B	\bar{A}	\bar{B}	\overline{AB}	$\overline{\bar{A} + \bar{B}}$
0	0	1	1	1	1
0	1	1	0	1	1
1	0	0	1	1	1
1	1	0	0	0	0

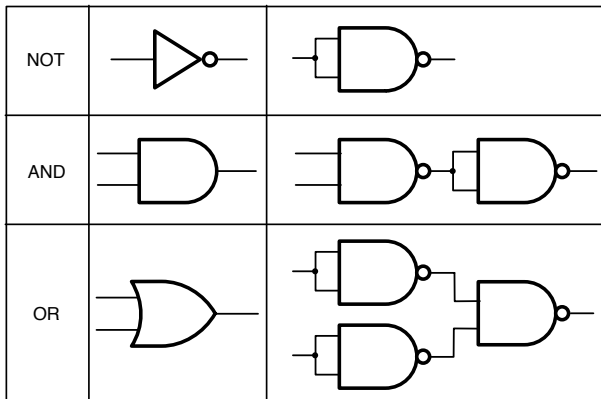


$$F = \overline{AB}$$



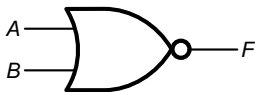
$$F = \overline{\bar{A} + \bar{B}}$$

NAND to Other Gates

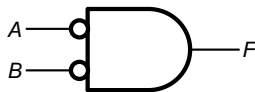


DeMorgan's Theorem Applied to NOR Gates

A	B	\bar{A}	\bar{B}	$\overline{A+B}$	$\overline{\bar{A} \cdot \bar{B}}$
0	0	1	1	1	1
0	1	1	0	0	0
1	0	0	1	0	0
1	1	0	0	0	0

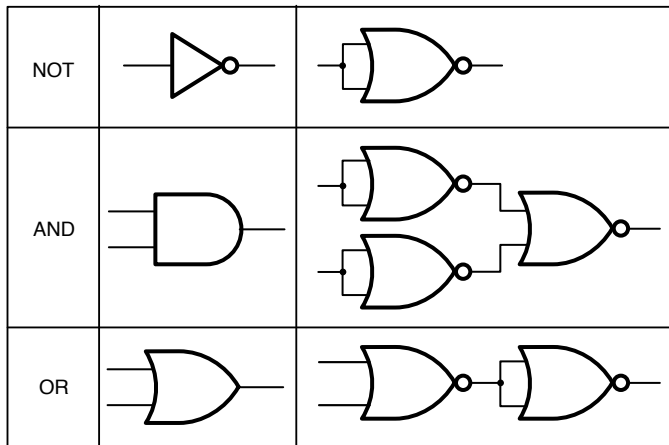


$$F = \overline{A+B}$$

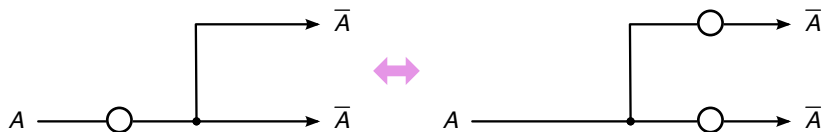


$$F = \overline{\bar{A} \cdot \bar{B}}$$

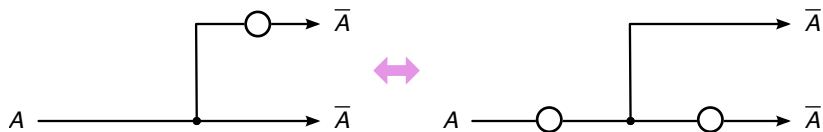
NOR to Other Gates



Pushing Bubbles

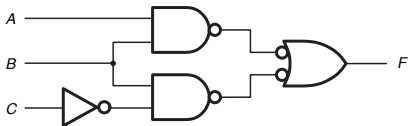
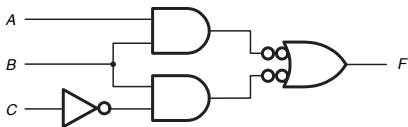
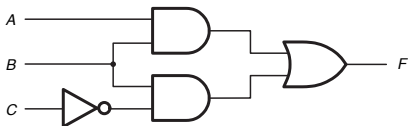


Pushing bubbles to the right.

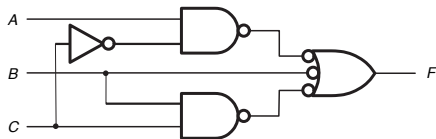
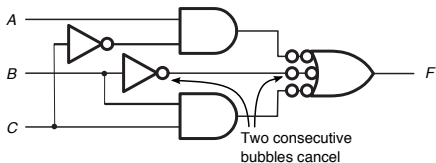
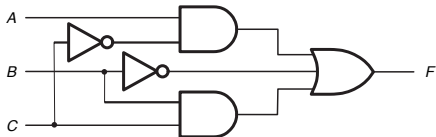


Pushing bubbles to the left.

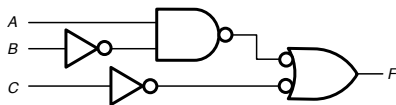
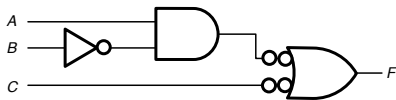
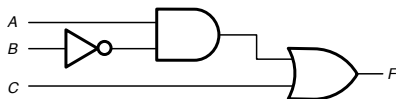
$F = AB + B\bar{C}$ Using only NAND and NOT



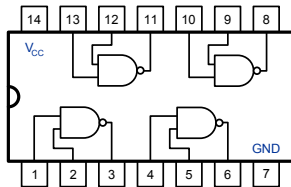
$F = \overline{A}C + \overline{B}C + BC$ Using only NAND and NOT



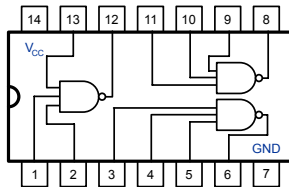
$F = A\bar{B} + C$ Using only NAND and NOT



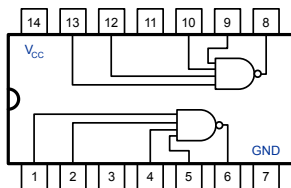
NAND Devices



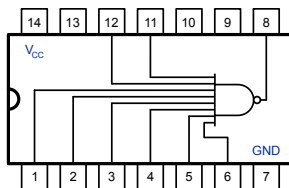
74x00



74x10

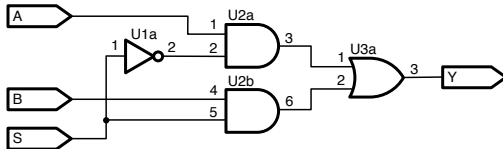
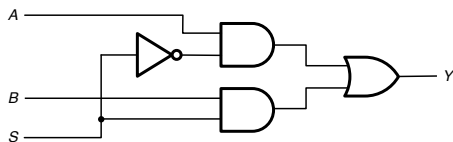


74x20

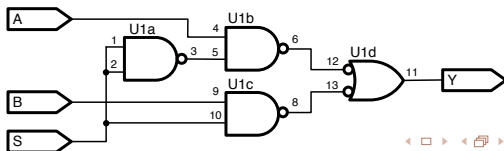
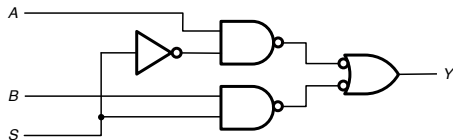
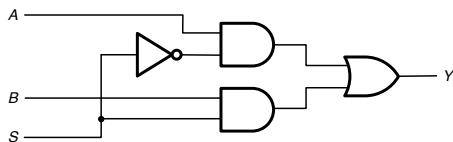


74x30

Using AND/OR/NOT: 3 chips



Using NAND: 1 chip only





<https://www.openlearning.com/courses/SKEE1223x>