

Chapter 9

Standard Combinational Circuits II

SKEE1223 Digital Electronics

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Overview

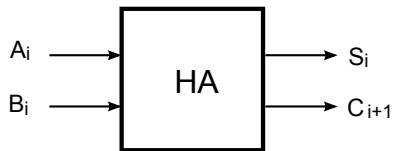
1 Adders

2 Comparators

3 Parity

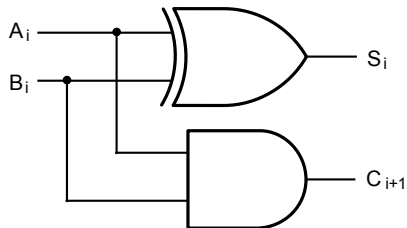
Half-Adder

| A_i | B_i | C_{i+1} | S_i |
|-------|-------|-----------|-------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |



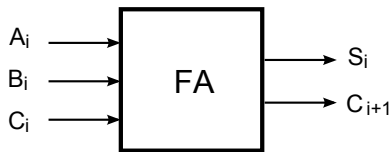
Half-Adder

$$\begin{aligned}C_{i+1} &= A_i B_i \\S_i &= \overline{A_i} B_i + A_i \overline{B_i} \\&= A_i \oplus B_i\end{aligned}$$



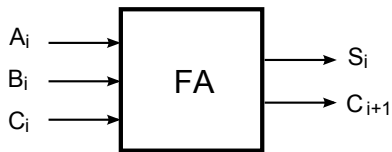
Full-Adder

| A_i | B_i | C_i | C_{i+1} | S_i |
|-------|-------|-------|-----------|-------|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |



Full-Adder

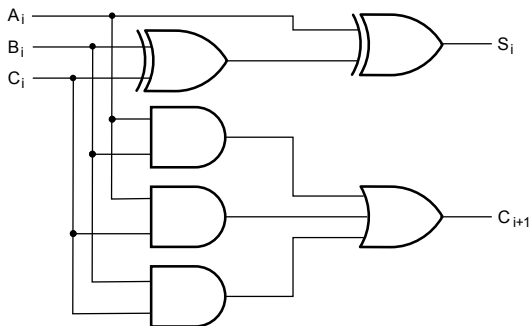
| A_i | B_i | C_i | C_{i+1} | S_i |
|-------|-------|-------|-----------|-------|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |



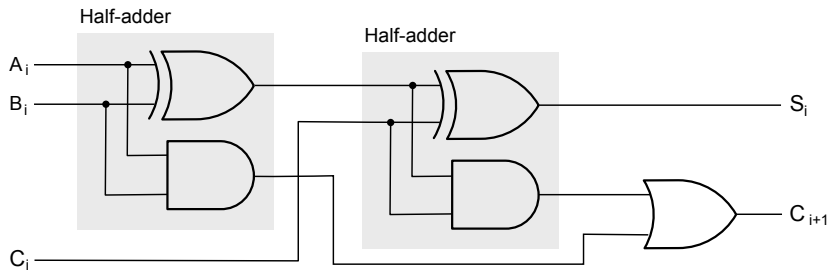
Full-Adder

$$C_{i+1} = A_i B_i + A_i C_i + B_i C_i$$

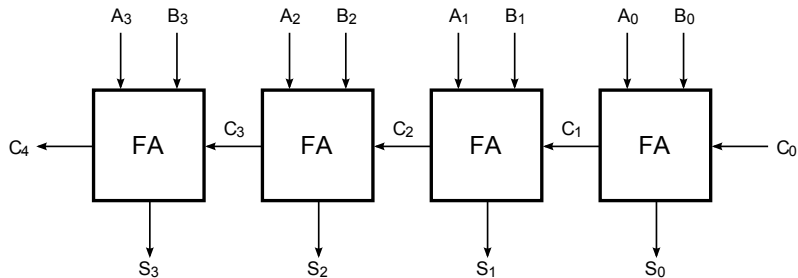
$$\begin{aligned} S_i &= \bar{A}_i \bar{B}_i C_i + \bar{A}_i B_i \bar{C}_i + A_i \bar{B}_i \bar{C}_i + A_i B_i C_i \\ &= A_i \oplus B_i \oplus C_i \end{aligned}$$



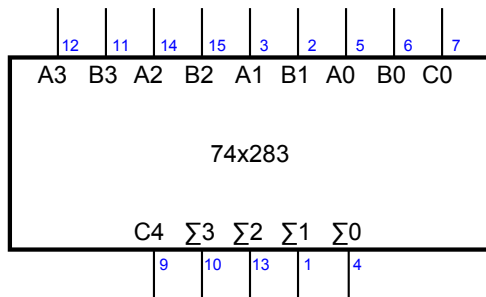
Full-Adder



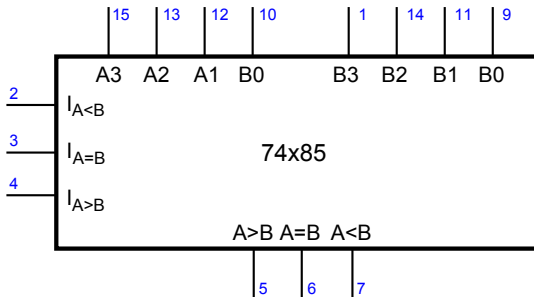
4-bit Ripple-Adder



74x283 Parallel Adder



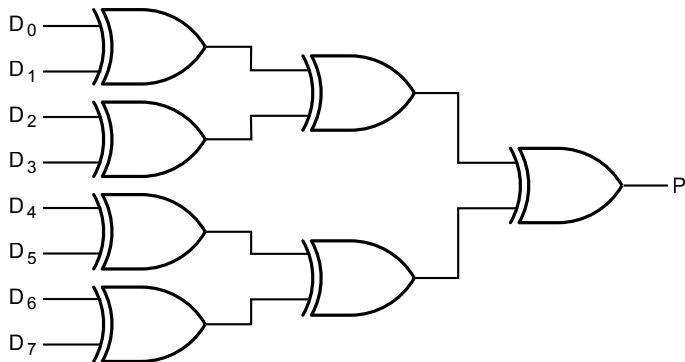
74x85 Parallel Comparator



74x85 Parallel Comparator

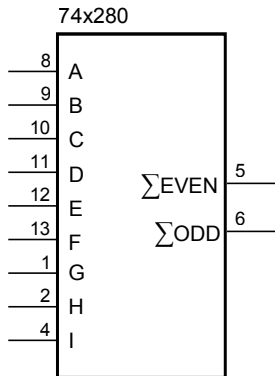
| Comparing Inputs | | | | Expression Inputs | | | Outputs | | |
|------------------|-------|-------|-------|-------------------|-----------|-----------|---------|-----|-----|
| A3,B3 | A2,B2 | A1,B1 | A0,B0 | $I_{A>B}$ | $I_{A<B}$ | $I_{A=B}$ | A>B | A<B | A=B |
| A3>B3 | × | × | × | × | × | × | H | L | L |
| A3<B3 | × | × | × | × | × | × | L | H | L |
| A3=B3 | A2>B2 | × | × | × | × | × | H | L | L |
| A3=B3 | A2<B2 | × | × | × | × | × | L | H | L |
| A3=B3 | A2=B2 | A1>B1 | × | × | × | × | H | L | L |
| A3=B3 | A2=B2 | A1<B1 | × | × | × | × | L | H | L |
| A3=B3 | A2=B2 | A1=B1 | A0>B0 | × | × | × | H | L | L |
| A3=B3 | A2=B2 | A1=B1 | A0<B0 | × | × | × | L | H | L |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | H | L | L | H | L | L |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | L | H | L | L | H | L |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | L | L | H | L | L | H |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | × | × | H | L | L | H |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | H | H | L | L | L | L |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | L | L | L | H | H | L |

Parity Generator



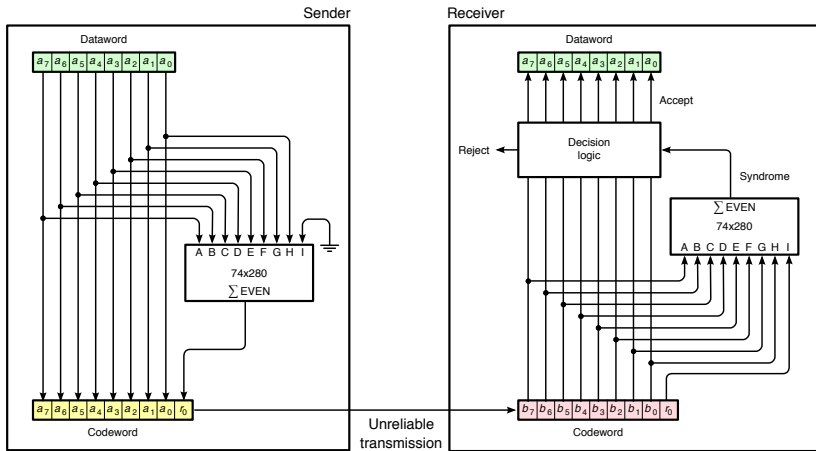
$$P = D_7 \oplus D_6 \oplus D_5 \oplus D_4 \oplus D_3 \oplus D_2 \oplus D_1 \oplus D_0$$

74x280 Parity Generator/Checker



| Number of High Inputs | Σ EVEN | Σ ODD |
|-----------------------|---------------|--------------|
| Even | 1 | 0 |
| Odd | 0 | 1 |

Application of Parity Generator/Checker





<https://www.openlearning.com/courses/SKEE1223x>