

# Chapter 12

## Standard Blocks: Registers

### SKEE1223 Digital Electronics

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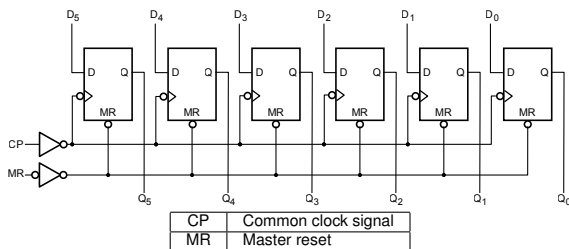
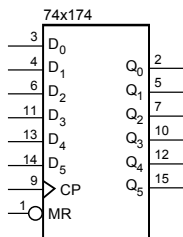
- 1 Overview
- 2 Registers
- 3 Shift Registers
- 4 Shift Register Chips
- 5 Shift Register Counters

# Sequential MSI

- Sequential MSI circuits are based on flip-flops.
- **Register:**
  - A register is a memory device that can be used to store more than one bit of information.
- **Counter:**
  - A register that is capable of incrementing or decrementing its contents.
- **Shift register:**
  - A register that shifts data from one flip-flop to the next

# Register

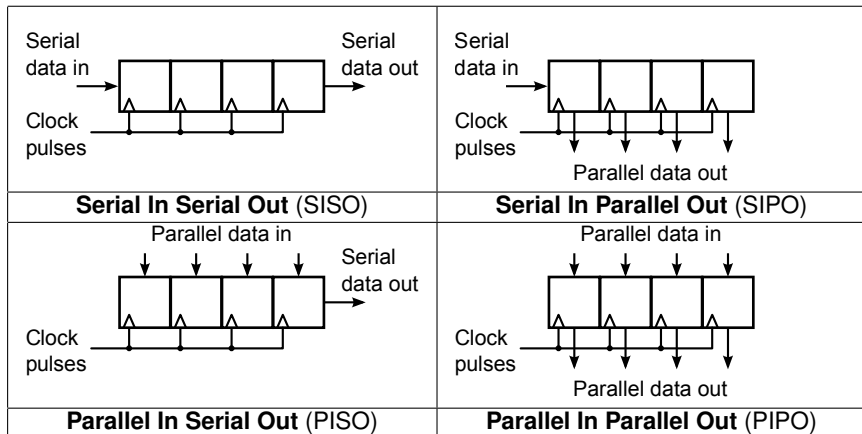
- Usually realized as several flip-flops with common control signals that control the movement of data to and from the register.



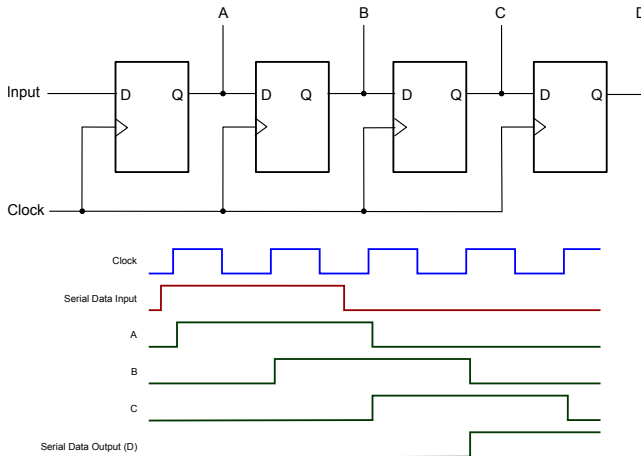
# Shift Registers

- Shift register: a register which can shift data left or right when a shift signal is applied.
- All flip-flops are driven by a common clock and common reset.
- Applications:
  - Producing time delay
  - Converting data from parallel to serial or vice versa.

# Data Movement in Shift Registers

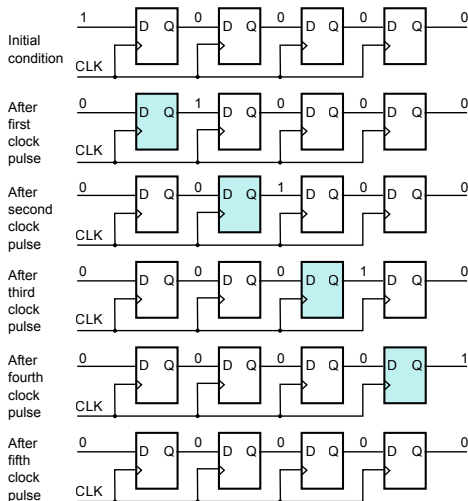


# A 4-bit SIPO Shift Register



Because of propagation delay, the value loaded into FF is the value of input before rising clock edge.

# Shift Register Animation

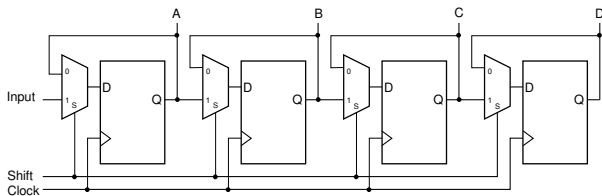




# Behavior of SIPO shift register in tabular form

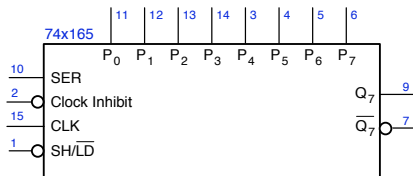
Clock #	Input	A+	B+	C+	D+
0	1	1	0	0	0
1	1	1	1	0	0
2	0	1	1	1	0
3	0	0	1	1	1
4	0	0	0	1	1
5	1	0	0	0	1
6	0	1	0	0	0

# A More Practical SIPO Shift Register



Shift = 0	Hold mode
Shift = 1	Shift mode

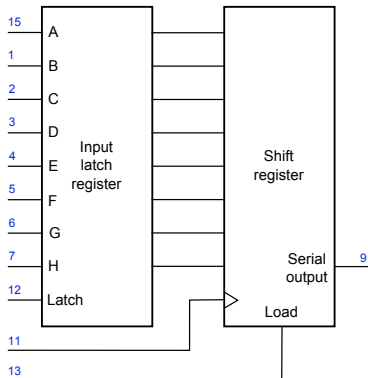
# 74x165 Parallel Load 8-bit Shift Register IC



SER	Serial data input
SH/LD	1 = shift, 0 = load
P0-P7	Parallel data inputs
Q7	Output of last flip-flop

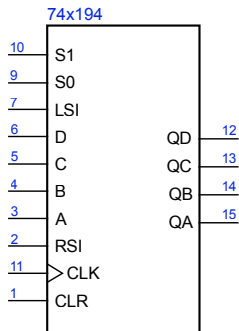
# 74x597 Parallel Load 8-bit Shift Register IC

Useful for adding input ports to microcontroller with limited pins.



A-H	Data input
Latch	Latch data into input latch register
Load	Transfer data into shift register
Clock	Shift data out
Serial output	Serial data to microcontroller

# 74x194 Multi-Function 4-bit Shift Register IC

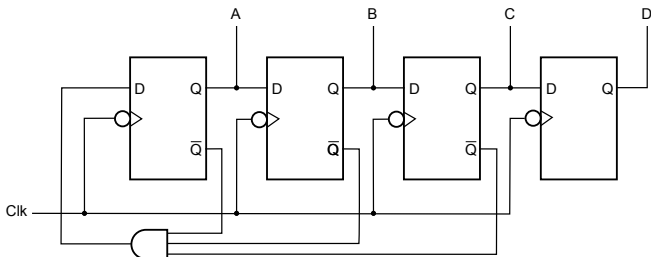


QD, QC, QB, QA	Parallel data output
D, C, B, A	Parallel data input
LSI	Left shift input
RSI	Right shift input
CLR	Reset all flip-flops
S1, S0	Mode control

S1	S0	Action	QA+	QB+	QC+	QD+
0	0	Hold	QA	QB	QC	QD
0	1	Shift right	RSI	QA	QB	QC
1	0	Shift left	QB	QC	QD	LSI
1	1	Load	A	B	C	D

# Ring Counter

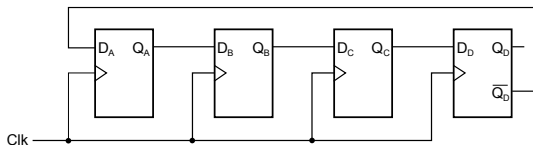
A ring counter is a circular shift register with only one flip-flop being set at any particular time; all others are cleared. The single bit is shifted from one flip-flop to the other to produce the sequence of timing signals.



QA+	QB+	QC+	QD+
1	0	0	0
0	1	0	0
0	0	1	0
0	0	0	1
1	0	0	0

# Johnson Counter

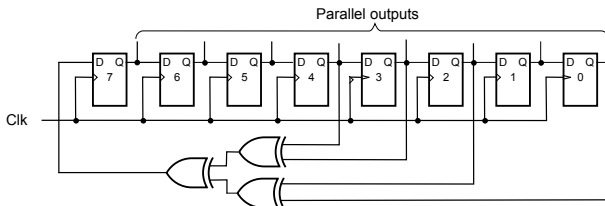
a.k.a. Twisted ring counter, is a variation of the ring counter, with the inverse output of the most significant flip-flop passed to the input of the least significant flip-flop.



QA+	QB+	QC+	QD+
1	0	0	0
1	1	0	0
1	1	1	0
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1
0	0	0	0
1	0	0	0

# Linear Feedback Shift Register

A shift register with a pseudo-random output sequence. Period of  $n$ -bit LFSR is  $2^n - 1$ .



Bits	Feedback polynomial
2	$x^2 + x + 1$
3	$x^3 + x^2 + 1$
4	$x^4 + x^3 + 1$
5	$x^5 + x^3 + 1$
6	$x^6 + x^5 + 1$
7	$x^7 + x^6 + 1$
8	$x^8 + x^6 + x^5 + x^4 + 1$