

# Chapter 13

## Standard Blocks: Counters

SKEE1223 Digital Electronics

Mun'im/Arif/Izam

FKE, Universiti Teknologi Malaysia

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## 1 Overview

## 2 Asynchronous Counters

## 3 Synchronous Counters

# Counter Overview

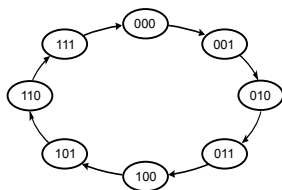
- A counter is a sequential machine that produces a specified count sequence. The count changes whenever the input clock is asserted.
- Implementation options:
  - **Clock:** Synchronous or Asynchronous
  - **Clock Trigger:** Positive edged or Negative edged
  - **Counts:** Binary, Decade
  - **Count Direction:** Up, Down, or Up/Down
  - **Flip-flops:** JK or T or D
  - **Specialty counters:** Shift register counters, counters with arbitrary sequence

# Counters

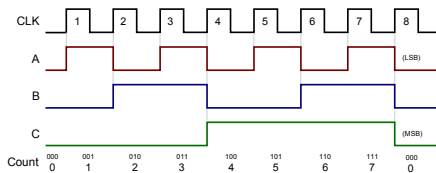
- **Synchronous counter:**
  - All state bits change synchronously when clock arrives
- **Asynchronous counter:**
  - Changing state bits are used as clocks to subsequent flip-flops → bits do not change at the same time
- For an  $n$ -bit counter, the count range is  $[0..2^n-1]$

3-bit Up Counter	3-bit Down Counter
000	000
001	111
010	110
011	101
100	100
101	011
110	010
111	001
000	000

# A 3-bit Counter

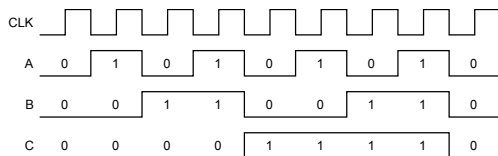
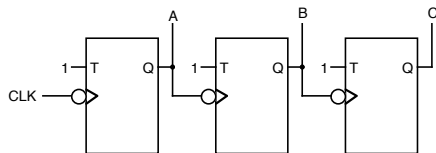


State diagram

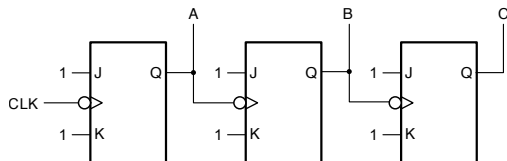


Timing Diagram

# Ripple Counters

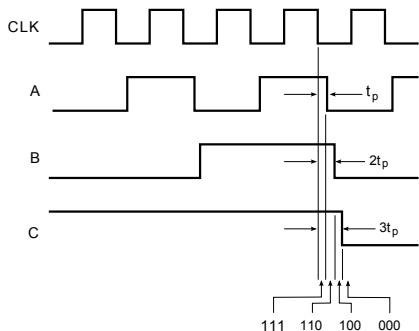


# Ripple Counters



- Output of any FF goes to clock input of next FF
- Each FF divides input frequency by 2:  $f_{in} = 2f_{out}$
- FF outputs change in ripple fashion, not at the same time
- Time for last output to stabilize limits max. counter speed
- Excellent when used as frequency divider
- Note: positive-edge triggered FF counts down

# Propagation Delay in Ripple Counters



## ■ Transient states:

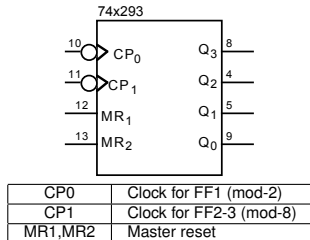
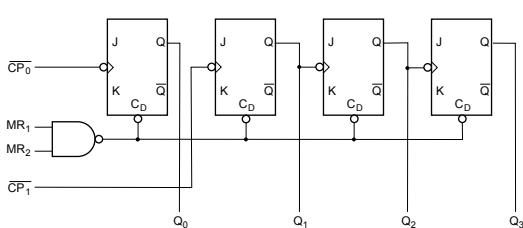
- state 111
- state 110 (flip-flop A toggles)
- state 100 (flip-flop B toggles)
- state 000 (flip-flop C toggles)

Max frequency for  $n$ -stage ripple counter:

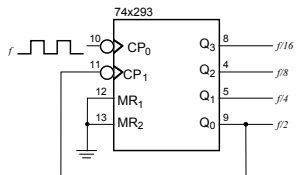
$$f = \frac{1}{T} \leq \frac{1}{nt_p}$$



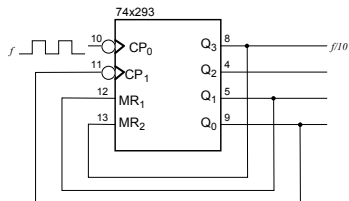
# 74x293 Ripple Counter IC



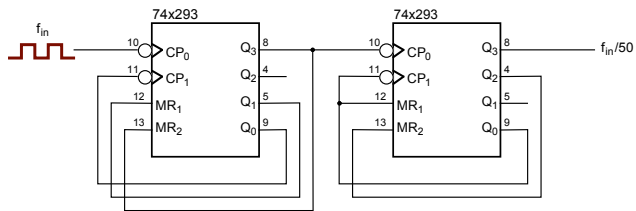
# 74x293 Ripple Counter IC



Mod-16 counter.

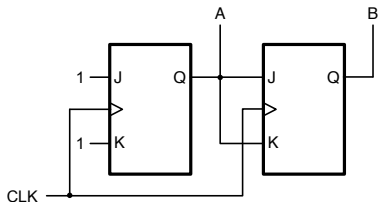


Mod-10 counter.

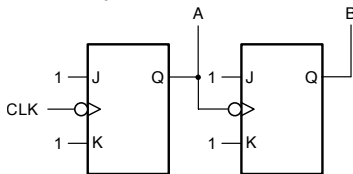


Mod-50 counter.

# Synchronous 2-bit Counter



Synchronous counter

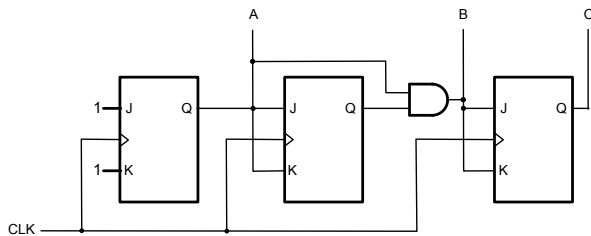


Asynchronous/ripple counter

Characteristics of Synchronous Counters:

- Common clock inputs
- Positive edge triggered FF
- Faster operation

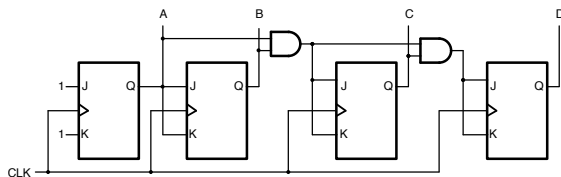
# Synchronous 3-bit Counter



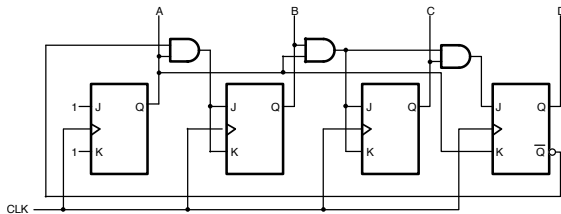
Mod-8 counter.

- For flip-flop delay  $t_f$  and worst case gate delay  $t_g$ :
  - Counter propagation delay =  $t_f + t_g$
  - Maximum frequency =  $\frac{1}{t_f + t_g}$

# Synchronous 4-bit Counters

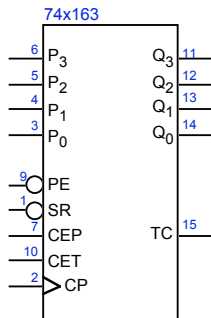


4-bit binary (mod-16) counter.



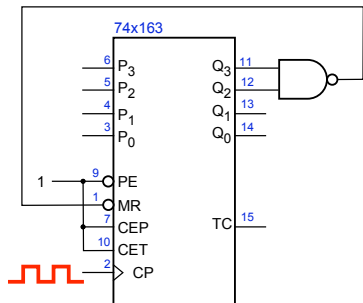
Decade (mod-10) counter.

# 74x163 4-bit Binary Counter IC

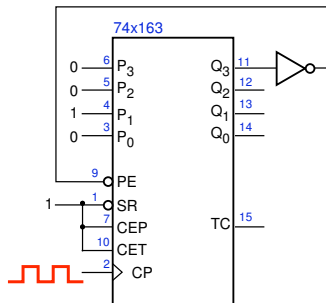


PE	Parallel load P0-P3 into counter
SR	Synchronous reset
CEP,CET	Count enable
TC	Terminal count (1 means count=1111)

# 74x163 4-bit Binary Counter IC

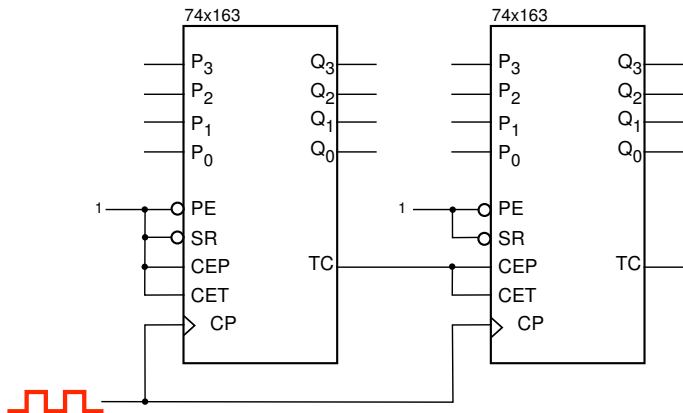


Mod-13 counter.



2..8 counter.

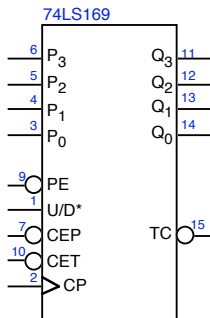
# 74x163 4-bit Binary Counter IC



Mod-256 counter.

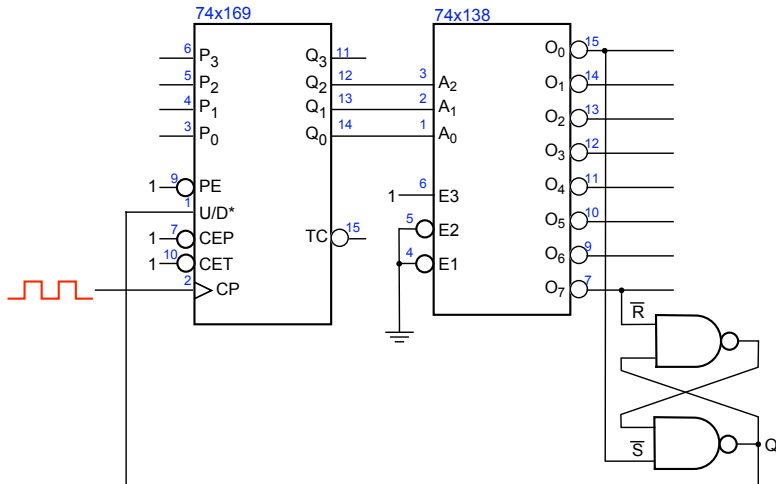


# 74x169 4-bit Binary Up/Down Counter IC



PE	Parallel load P0-P3 into counter
U/D*	1 = Count up, 0 = Count down
CEP,CET	Count enable
TC	Terminal count: 0 means count=1111 counting up count=0000 counting down

# 74x163 as Left/Right Running Light





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