

# Chapter 2

## Combinational Circuits

### SKEE2263 Digital Systems

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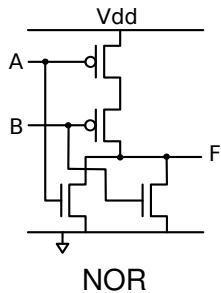
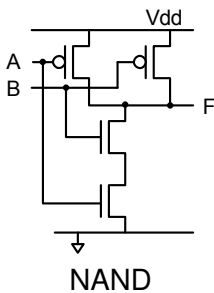
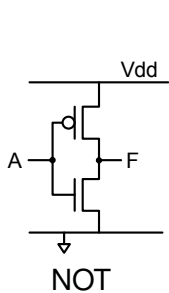
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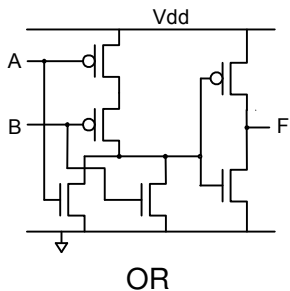
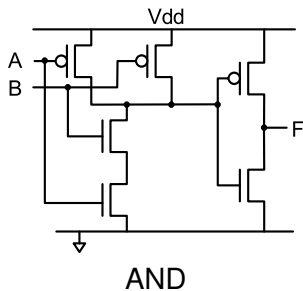
# Why CMOS?

- Most logic design today is done on CMOS circuits
- Most important characteristics:
  - High noise immunity
  - Low static power consumption

# CMOS Gates



# CMOS Gates



# CMOS Power Considerations

- CMOS power consumption increases with switching frequency
- Reducing power consumption increases CMOS circuit reliability and increases design flexibility
- CMOS Power Expression:

$$P_{\text{total}} = P_s + P_d$$

where:

$P_{\text{total}}$  = total power

$P_s$  = static power

$P_d$  = dynamic power

## CMOS Static Power

- Static power or quiescent power consumption ( $P_s$ ) is the power drawn when the device is powered up and there no signal at the input.
- The dissipation comes mainly by leakage through the diodes. In CMOS,  $P_s$  is extremely small.

$$P_s = I_{dd} \cdot V_{dd}$$

where:

$V_{dd}$  = Supply Voltage (V)

$I_{dd}$  = Leakage current (A)

# CMOS Dynamic Power

- Dynamic power = transient power ( $P_t$ ) + capacitive load power ( $P_c$ ).
- **Transient power** or dynamic short-circuit power consumption is the amount of consumed when the device changes logic states from one logic state to another.
- **Capacitive-load power consumption** is the power consumed in charging external load capacitances

# CMOS Dynamic Power

$$\begin{aligned}P_{\text{dynamic}} &= P_t + P_c \\ &= (C_L + C) \cdot V_{\text{dd}}^2 \cdot f \cdot N^3\end{aligned}$$

where:

$C_L$  = Load capacitance ( $F$ )

$C$  = Internal capacitance ( $F$ )

$V_{\text{dd}}$  = Supply voltage ( $V$ )

$f$  = Switching frequency ( $Hz$ )

$N$  = Number of bits that are switching



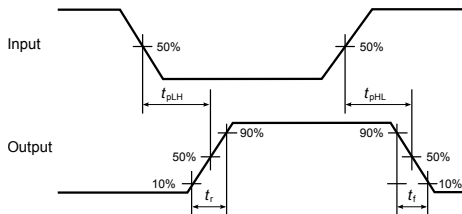
# Importance of Propagation Delay

- A real logic gate does not respond to a change on one of its inputs instantaneously.
- The propagation delay of a logic circuit can be used to define:
  - When the output of the logic circuit is valid.
  - The maximum speed of a combinational logic circuit.
  - The maximum frequency of a sequential logic circuit.

# Propagation Delay Values

$t_{PHL}$  – delay from an input is given to the time the output changes from high to low.

$t_{PLH}$  – delay from an input is given to the time the output changes from low to high.



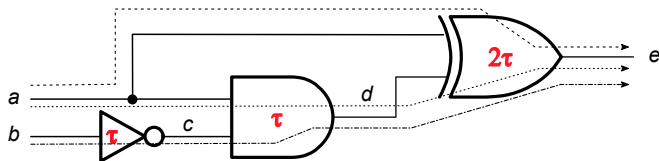
■ Propagation delay – average of  $t_{PHL}$ ,  $t_{PLH}$ :

$$t_{pd} = \frac{t_{PHL} + t_{PLH}}{2}$$

# Critical Path

## Critical Path

Path that causes the longest delay.



Path	Delay
$a - e$	$2\tau$
$a - d - e$	$3\tau$
$b - c - d - e$	$4\tau$ $\leftarrow$ Critical path delay

## Normalized CMOS Gate Delays (VLSI Extra Slide)

Not is syllabus. Just to give an idea that gate delay is not so simple to derive.

Gate	Delay	Area	Comment
Inverter	1	1	Minimum delay
2-input NOR	1	3	More area to produce delay equal to that of an inverter
2-input NAND	1	3	More area to produce delay equal to that of an inverter
2-input OR	2	4	Composed of NOR followed by inverter
2-input AND	2	4	Composed of NAND followed by inverter
2-input XOR	3	11	Built using inverters and NAND gates
$n$ -input OR	2	$n/3+2$	Uses saturated load ( $n > 2$ )
$n$ -input AND	3	$4n/3+2$	Uses $n$ -input OR preceded by inverters ( $n > 2$ )

# Glitches and Hazards

## Glitches:

- Unwanted transitions
- Caused by propagation delay
- Happens when an input changes state, and the signal takes two or more paths through the circuit and one path has a longer delay than other

## Hazards:

- Related to glitches
- A **hazard** is a characteristic of a digital circuit: a circuit with a hazard may produce a glitch

# Kinds of Hazards

## Static hazards :

- **Static-0 hazard** – when the output should remain at 0 but experiences an unwanted 1-pulse.
- **Static-1 hazard** – when the output should remain at 1 but experiences an unwanted 0-pulse.

## Dynamic hazard;

- when a single input variable change causes not a single change at the output but multiple changes before settling at the new value

# Kinds of Hazards



Static-0 hazard.

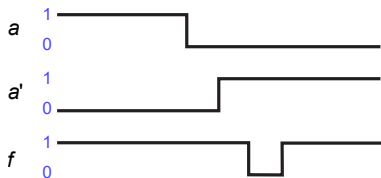
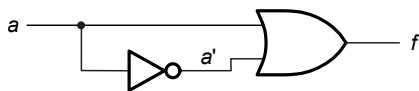


Static-1 hazard.



Dynamic hazard.

## Circuit with Static Hazard

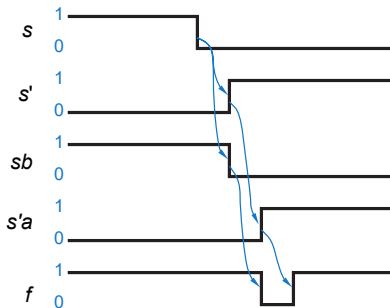
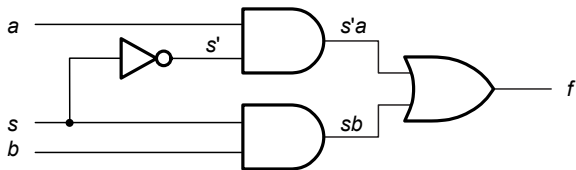




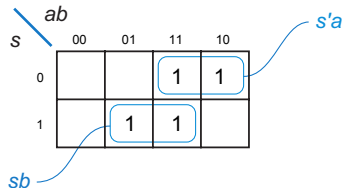
# Eliminating Hazards

- Insert another delay to the circuit.
- Re-clock the final output signals.
- Insert a redundant term in the form of an additional gate.

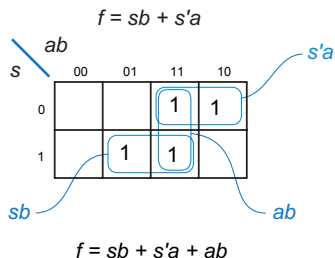
## Circuit with Static Hazard



# Eliminating Hazards



K-map for original circuit.



K-map for modified circuit.

# Eliminating Hazards

