Chapter 2
Combinational Circuits
SKEE2263 Digital Systems

Mun'im Zabidi {munim@utm.my}
Ismahani Ismail {ismahani@fke.utm.my}
Izam Kamisian {e-izam@utm.my}

Faculty of Electrical Engineering, Universiti Teknologi Malaysia

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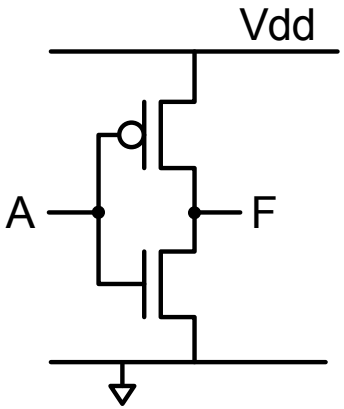
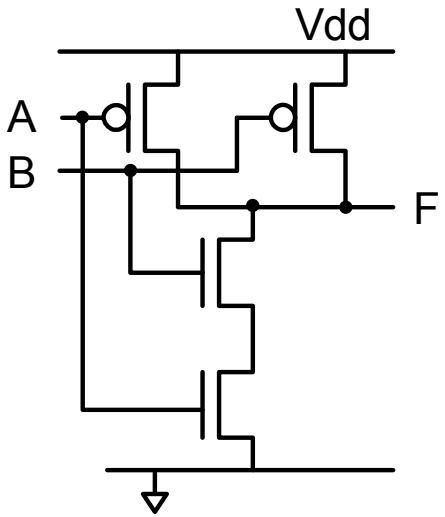
Why CMOS?

- Most logic design today is done on CMOS circuits
- Most important characteristics:
  - High noise immunity
  - Low static power consumption

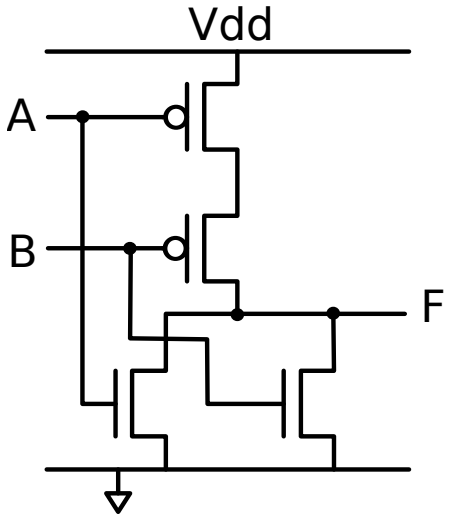
CMOS Gates



NOT

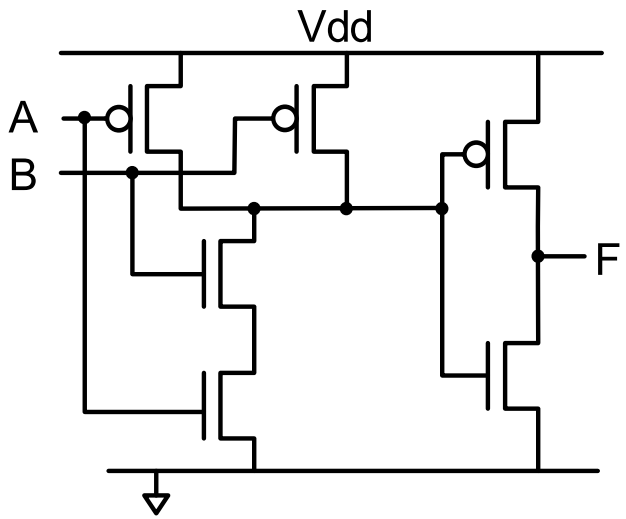


NAND

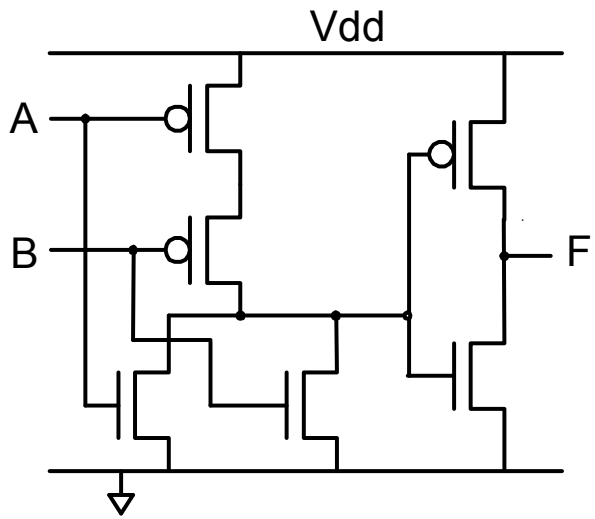


NOR

CMOS Gates



AND



OR

CMOS Power Considerations

- CMOS power consumption increases with switching frequency
- Reducing power consumption increases CMOS circuit reliability and increases design flexibility
- CMOS Power Expression:

$$P_{\text{total}} = P_{\text{s}} + P_{\text{d}}$$

where:

$$P_{\text{total}} = \text{total power}$$
$$P_{\text{s}} = \text{static power}$$
$$P_{\text{d}} = \text{dynamic power}$$

CMOS Static Power

- Static power or quiescent power consumption (P_{s}) is the power drawn when the device is powered up and there no signal at the input.
- The dissipation comes mainly by leakage through the diodes. In CMOS, P_{s} is extremely small.

$$P_{\mathrm{s}} = I_{\mathrm{dd}} \cdot V_{\mathrm{dd}}$$

where:

$$V_{\mathrm{dd}} = \text{Supply Voltage (V)}$$
$$I_{\mathrm{dd}} = \text{Leakage current (A)}$$

CMOS Dynamic Power

- Dynamic power = transient power (P_t) + capacitive load power (P_c).
- **Transient power** or dynamic short-circuit power consumption is the amount of consumed when the device changes logic states from one logic state to another.
- **Capacitive-load power consumption** is the power consumed in charging external load capacitances

CMOS Dynamic Power

$$\begin{aligned} P_{\text{dynamic}} &= P_t + P_c \\ &= (C_L + C) \cdot V_{\text{dd}}^2 \cdot f \cdot N^3 \end{aligned}$$

where:

$$\begin{aligned} C_L &= \text{Load capacitance } (F) \\ C &= \text{Internal capacitance } (F) \\ V_{\text{dd}} &= \text{Supply voltage } (V) \\ f &= \text{Switching frequency } (Hz) \\ N &= \text{Number of bits that are switching} \end{aligned}$$

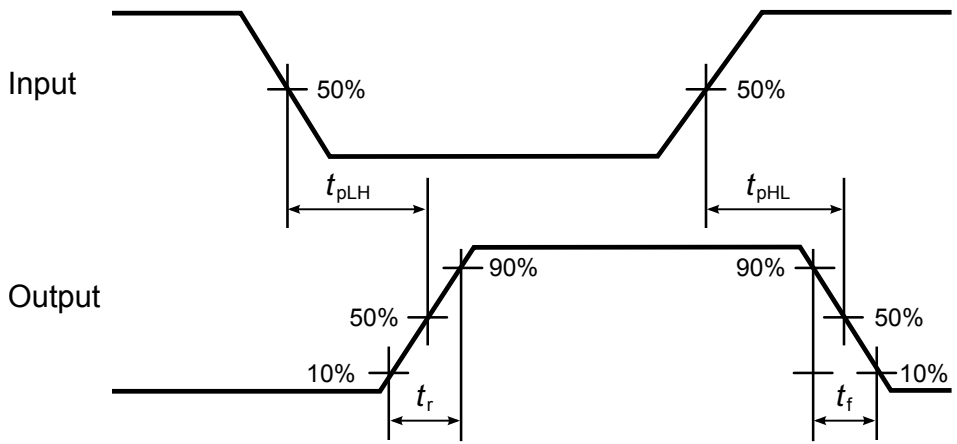
Importance of Propagation Delay

- A real logic gate does not respond to a change on one of its inputs instantaneously.
- The propagation delay of a logic circuit can be used to define:
  - When the output of the logic circuit is valid.
  - The maximum speed of a combinational logic circuit.
  - The maximum frequency of a sequential logic circuit.

Propagation Delay Values

t_{PHL} – delay from an input is given to the time the output changes from high to low.

t_{PLH} – delay from an input is given to the time the output changes from low to high.



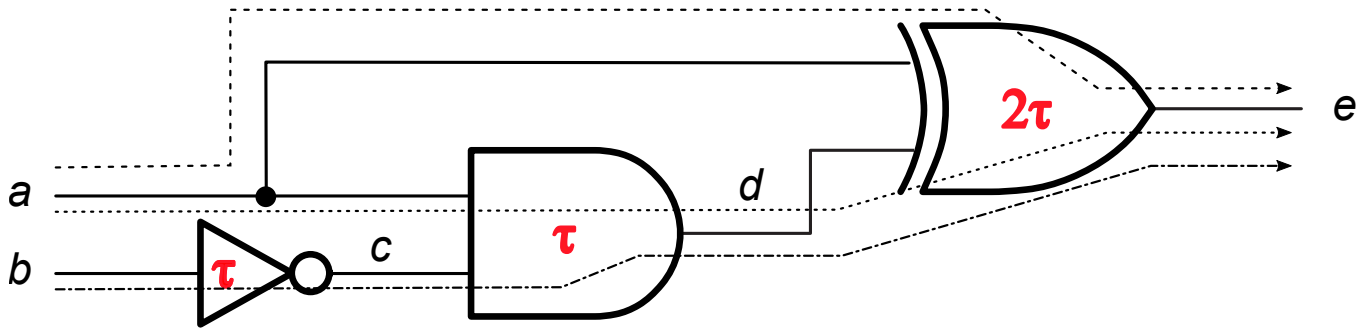
- **Propagation delay** – average of t_{PHL}, t_{PLH}:

$$t_{pd} = \frac{t_{\mathrm{PHL}} + t_{\mathrm{PLH}}}{2}$$

Critical Path

Critical Path

Path that causes the longest delay.



Path	Delay	
a - e	2τ	
a - d - e	3τ	
b - c - d - e	4τ	$\Leftarrow$ Critical path delay

Normalized CMOS Gate Delays (VLSI Extra Slide)

Not is syllabus. Just to give an idea that gate delay is not so simple to derive.

Gate	Delay	Area	Comment
Inverter	1	1	Minimum delay
2-input NOR	1	3	More area to produce delay equal to that of an inverter
2-input NAND	1	3	More area to produce delay equal to that of an inverter
2-input OR	2	4	Composed of NOR followed by inverter
2-input AND	2	4	Composed of NAND followed by inverter
2-input XOR	3	11	Built using inverters and NAND gates
n-input OR	2	n/3+2	Uses saturated load ($n > 2$)
n-input AND	3	4n/3+2	Uses n-input OR preceded by inverters ($n > 2$)

Source: `http://www.ece.uvic.ca/~fayez/courses/ceng465/lab_465/project1/adders.pdf`

Glitches and Hazards

Glitches:

- Unwanted transitions
- Caused by propagation delay
- Happens when an input changes state, and the signal takes two or more paths through the circuit and one path has a longer delay than other

Hazards:

- Related to glitches
- A **hazard** is a characteristic of a digital circuit: a circuit with a hazard may produce a glitch

Kinds of Hazards

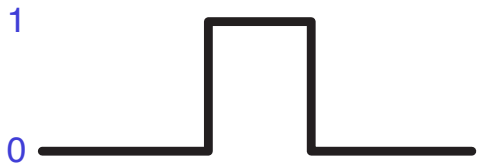
Static hazards :

- **Static-0 hazard** – when the output should remain at 0 but experiences an unwanted 1-pulse.
- **Static-1 hazard** – when the output should remain at 1 but experiences an unwanted 0-pulse.

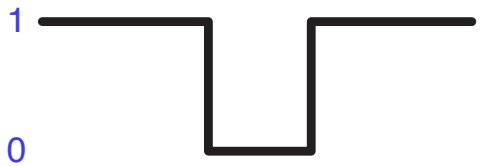
Dynamic hazard;

- when a single input variable change causes not a single change at the output but multiple changes before settling at the new value

Kinds of Hazards



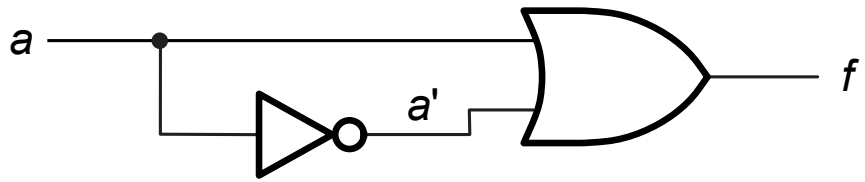
Static-0 hazard.

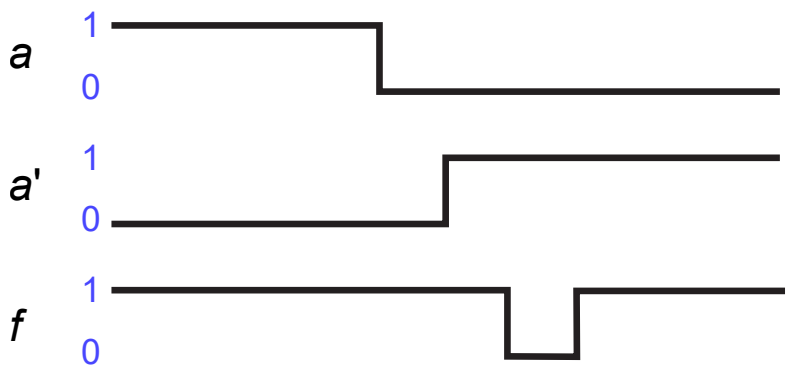


Static-1 hazard.

Dynamic hazard.

Circuit with Static Hazard

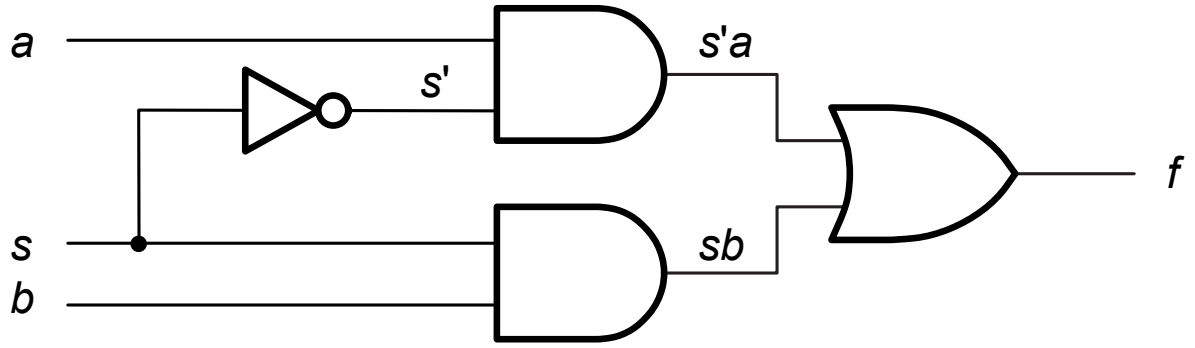


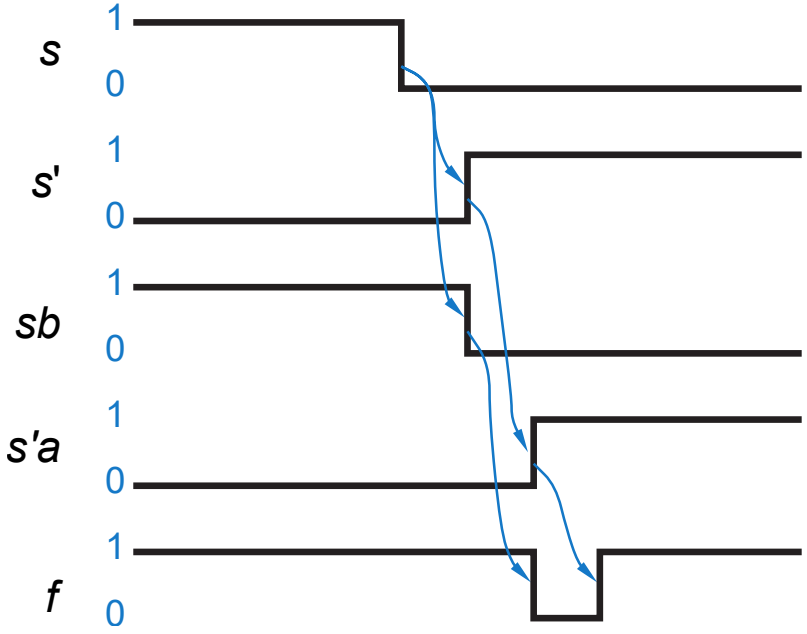


Eliminating Hazards

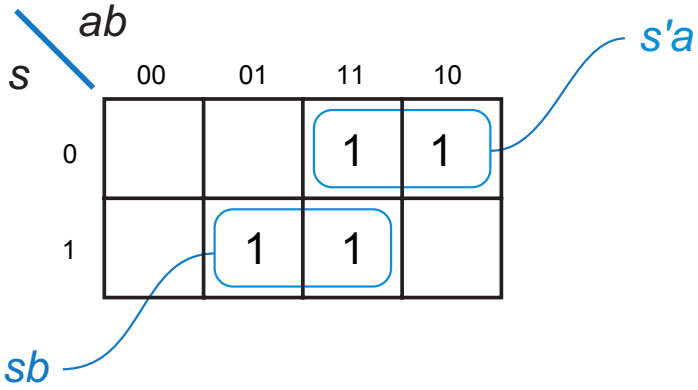
- Insert another delay to the circuit.
- Re-clock the final output signals.
- Insert a redundant term in the form of an additional gate.

Circuit with Static Hazard



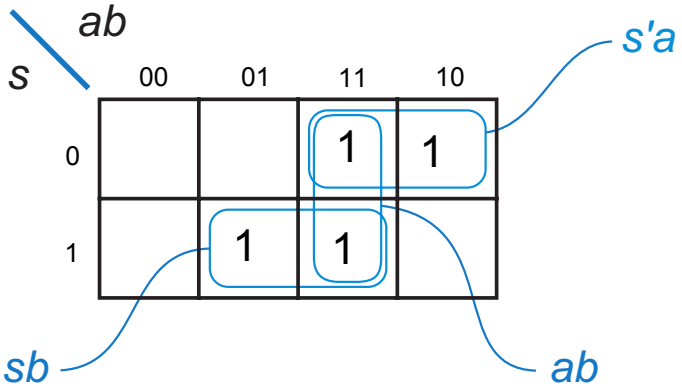


Eliminating Hazards



$f = sb + s'a$

K-map for original circuit.



$f = sb + s'a + ab$

K-map for modified circuit.

Eliminating Hazards