Chapter 7
Sequential Logic
SKEE2263 Digital Systems

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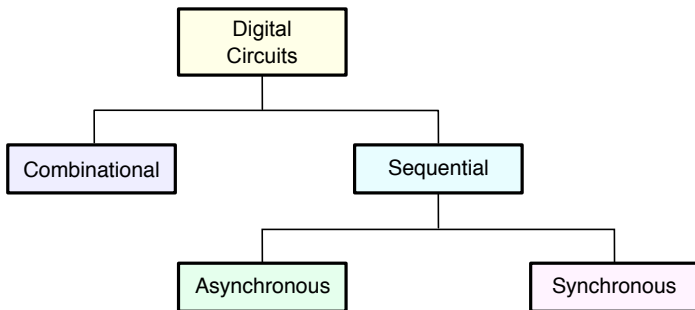
February 10, 2018
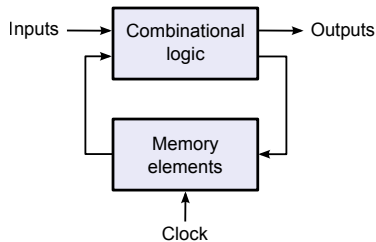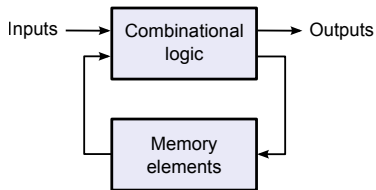
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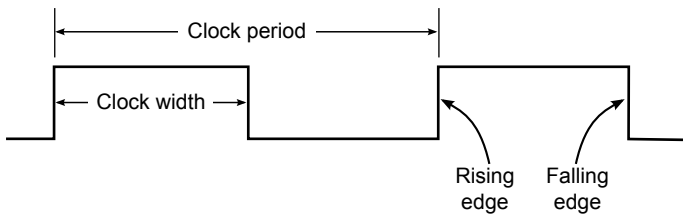## Classes of Digital Circuits

Sequential vs Combinational

- Combinational:
    - Output = f(Present Input)
    - Memoryless
- Sequential:
    - Output = f(Present Input, Past Input)
    - Uses latches/flip-flop as memory
    - May have clock input (synchronous) or not (asynchronous)

Clocks

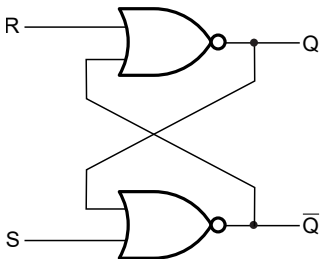- Asynchronous sequential circuits have no clock input
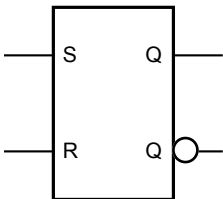
Clock Parts

SR Latch: Gate Level

- Bistable circuits: stable in state 0 or 1
- Simplest bistable is SR latch

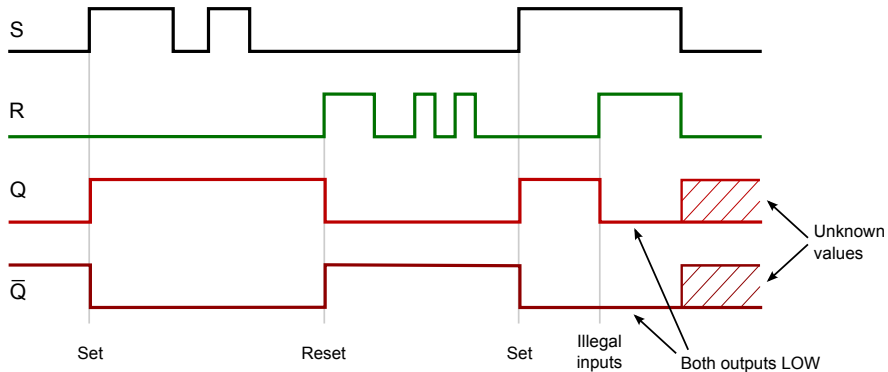# SR Latch: Logic Symbol, Characteristic Table

S	R	Q^+	$\overline{Q}^+$	Action
0	0	Q	$\overline{Q}$	No change
0	1	0	1	Reset
1	0	1	0	Set
1	1	0	0	Forbidden

SR Latch: Timing Diagram

$\overline{S}\,\overline{R}$ Latch: Gate Level, Characteristic Table
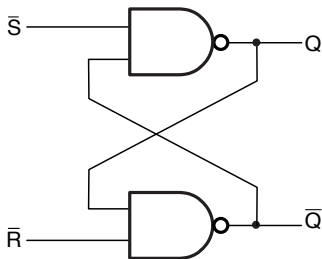
S	R	Q^+	$\overline{Q}^+$	Action
0	0	1	1	Forbidden
0	1	1	0	Set
1	0	0	1	Reset
1	1	Q	$\overline{Q}$	No change

Gated SR Latch: Logic Symbol, Characteristic Table
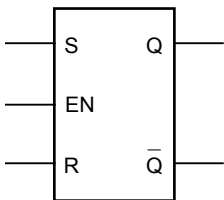
EN	S	R	Q^+	Action
0	$\times$	$\times$	Q	No change
1	0	0	Q	No change
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	$\times$	Forbidden

Gated SR Latch: Timing Diagram
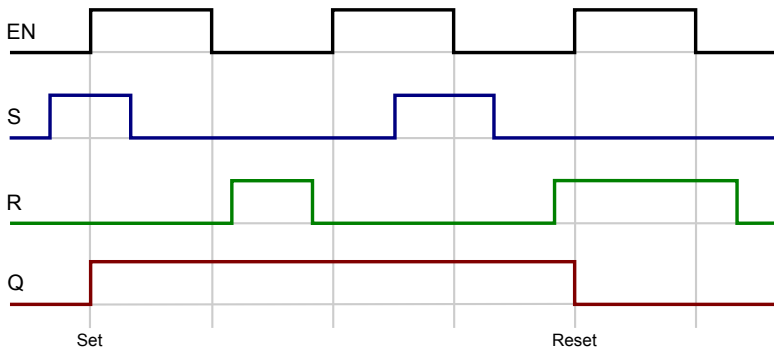
Gated D Latch: Logic Symbol, Characteristic Table
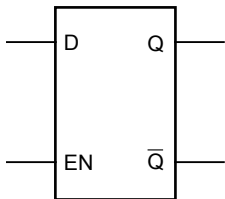
EN	**D**	**Q**$^{+}$	**Action**
0	$\times$	Q	Storage state
1	0	0	Transparent mode
1	1	1	Transparent mode

Gated D Latch: Timing Diagram
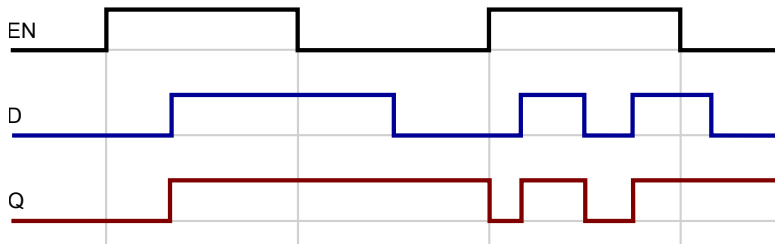
D Flip-Flop: Logic Symbol, Characteristic Table
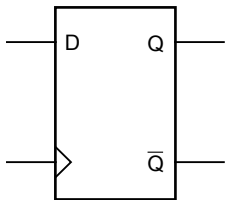
Clk	D	Q$^+$	Action
0	$\times$	Q	No change
1	$\times$	Q	No change
↑	0	0	Reset
↑	1	1	Set

D Flip-Flop vs Latch
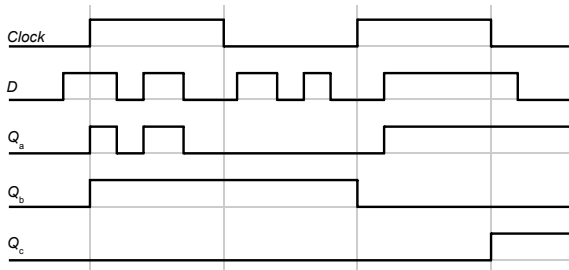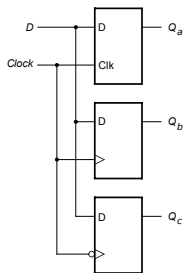
JK Flip-Flop: Logic Symbol, Characteristic Table
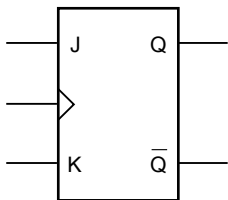
Clk	J	K	Q^+	Action
0	$\times$	$\times$	Q	No change
1	$\times$	$\times$	Q	No change
$\uparrow$	0	0	Q	No change
$\uparrow$	0	1	0	Reset
$\uparrow$	1	0	1	Set
$\uparrow$	1	1	Q'	Toggle

T Flip-Flop: Logic Symbol, Characteristic Table
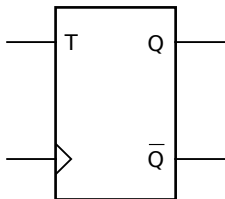
Clk	T	Q$^+$	Action
0	$\times$	Q	No change
1	$\times$	Q	No change
↑	0	Q	No change
↑	1	Q'	Toggle

FF Timing Parameters
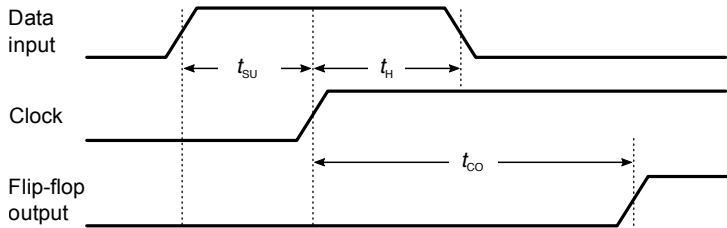
FF Timing Parameters

Setup time, t_{SU} – the minimum time that a flip-flop input must be stable before the clock edge.

Hold time, t_{H} – the minimum time after the clock edge that a flip-flop input must continue to be in the same stable state.

Clock to output delay time, t_{CO} – the minimum time after a clock edge to obtain a valid output

Setup Time Violation
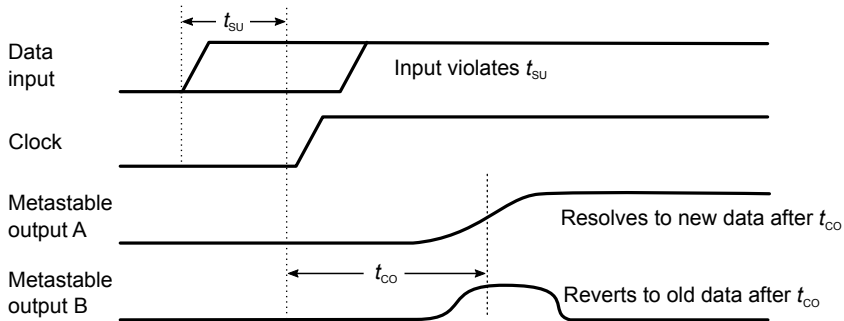
Causes of Metastability

Asynchronous Inputs.

Data transfer across clock domains.

What Happens During Metastability
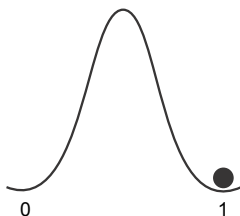
Stable state 0   Stable state 1   Metastable state
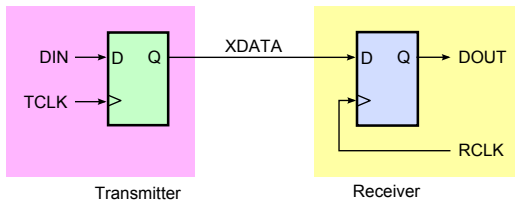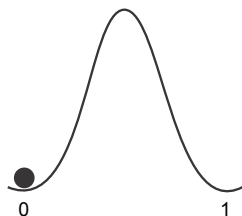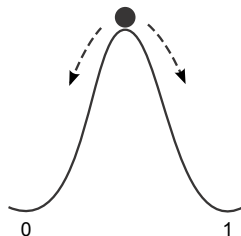
Solution for Metastability

Asynchronous input / Metastable signal / Synchronous signal / Synchronous system / CLK / Two-stage synchronizer
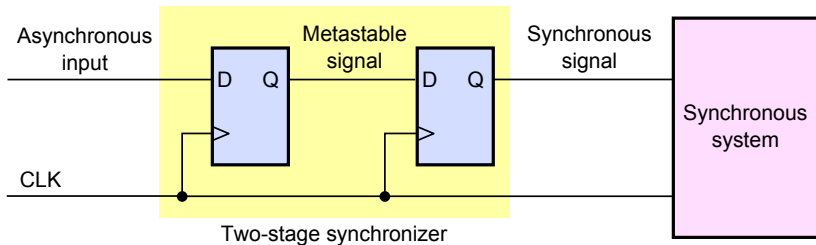
D Flip-Flop

Characteristic table:

D	Q^+	Operation
0	0	Reset
1	1	Set

Excitation table:

Present State Q	Next State Q^+	Input D
0	0	0
0	1	1
1	0	0
1	1	1

State diagram:
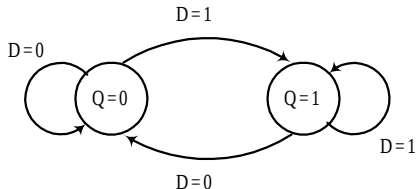
Characteristic Equation:

$$Q^+ = D$$

T Flip-Flop

Characteristic table:

T	Q^+	Operation
0	Q	No change
1	Q'	Complement

Excitation table:

Present State Q	Next State Q^+	Input T
0	0	0
0	1	1
1	0	1
1	1	0

State diagram:
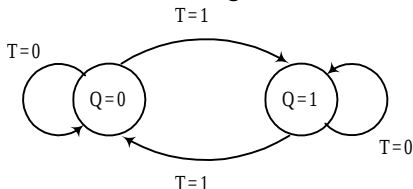
Characteristic Equation:

$$Q^+ = T'Q + TQ' = T \oplus Q$$

JK Flip-Flop

Characteristic table:

J	K	Q^+	Operation
0	0	Q	No change
0	1	0	Reset
1	0	1	Set
1	1	Q'	Complement

Excitation table:

Present State Q	Next State Q^+	Inputs J	K
0	0	0	$\times$
0	1	1	$\times$
1	0	$\times$	1
1	1	$\times$	0

Characteristic Equation:

$$Q^+ = J\overline{Q} + \overline{K}Q$$

State diagram:

JK=10 or 11

JK=00 or 01

Q=0   Q=1

JK=00 or 10

JK=01 or 11
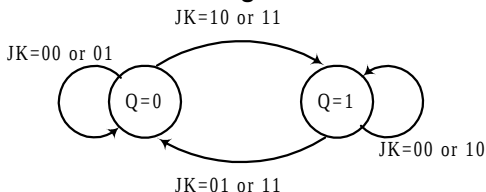
SR Flip-Flop

Characteristic table:

S	R	Q^+	Operation
0	0	Q	No change
0	1	0	Reset
1	0	1	Set
1	1	?	Undefined

Excitation table:

Present State Q	Next State Q^+	Inputs S	R
0	0	0	$\times$
0	1	1	0
1	0	0	1
1	1	$\times$	0

State diagram:

Characteristic Equation:

$$Q^+ = S + \overline{R}Q$$
$$SR \neq 1$$

$SR=10$

$SR=00$ or 01

$Q=0$ $Q=1$

$SR=00$ or 10

$SR=01$
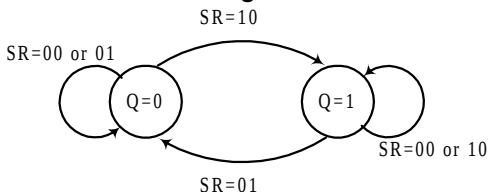
Excitation Table Summary

Q	Q$^+$	S	R	D	J	K	T
0	0	0	$\times$	0	0	$\times$	0
0	1	1	0	1	1	$\times$	1
1	0	0	1	0	$\times$	1	1
1	1	$\times$	0	1	$\times$	0	0