Chapter 8
Registers
SKEE2263 Digital Systems

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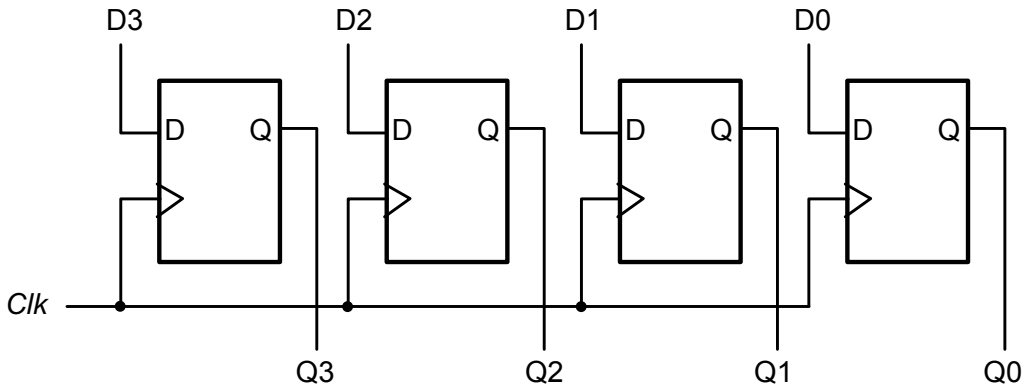
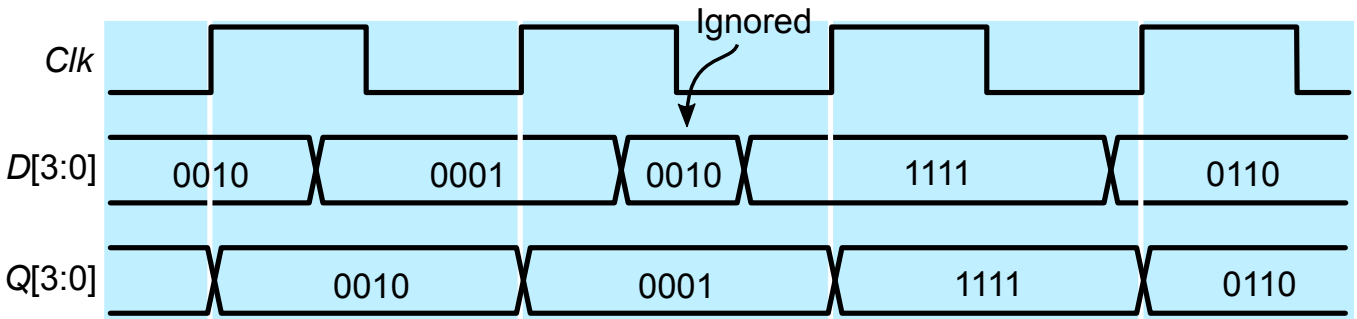
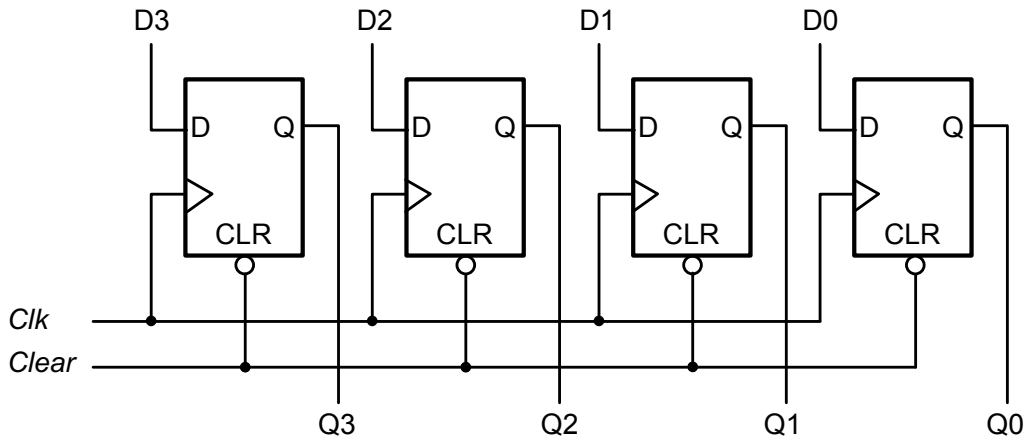
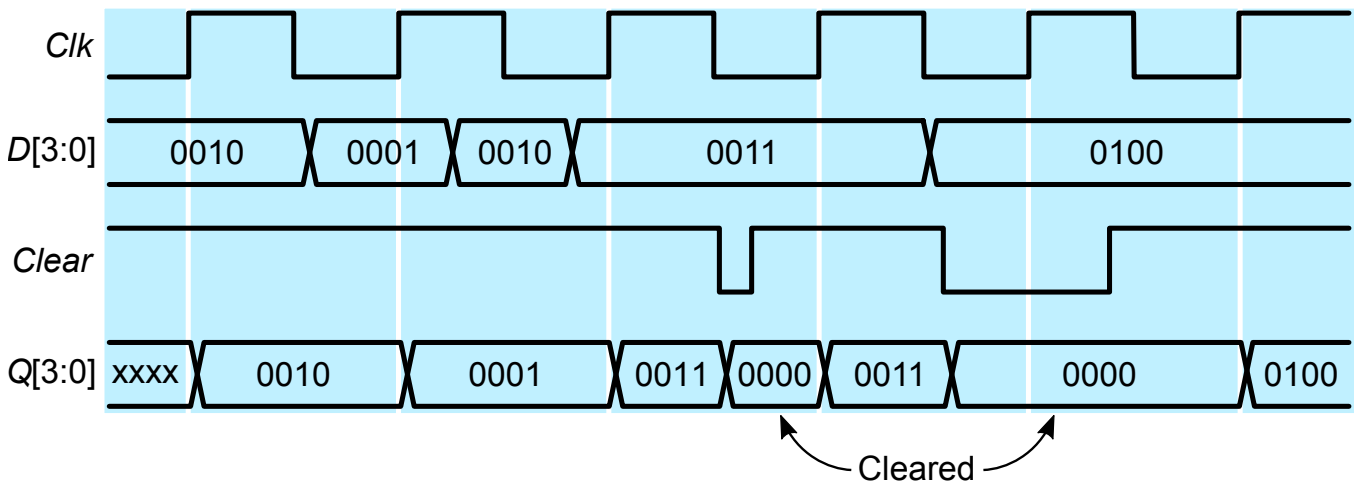
Basic Register



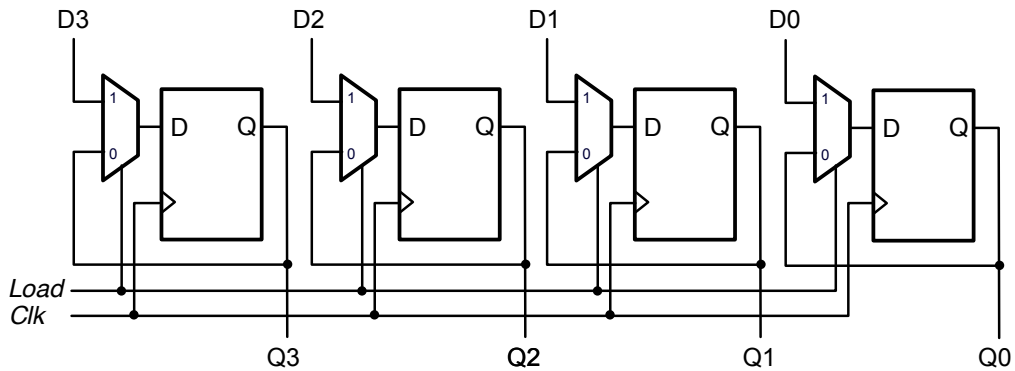


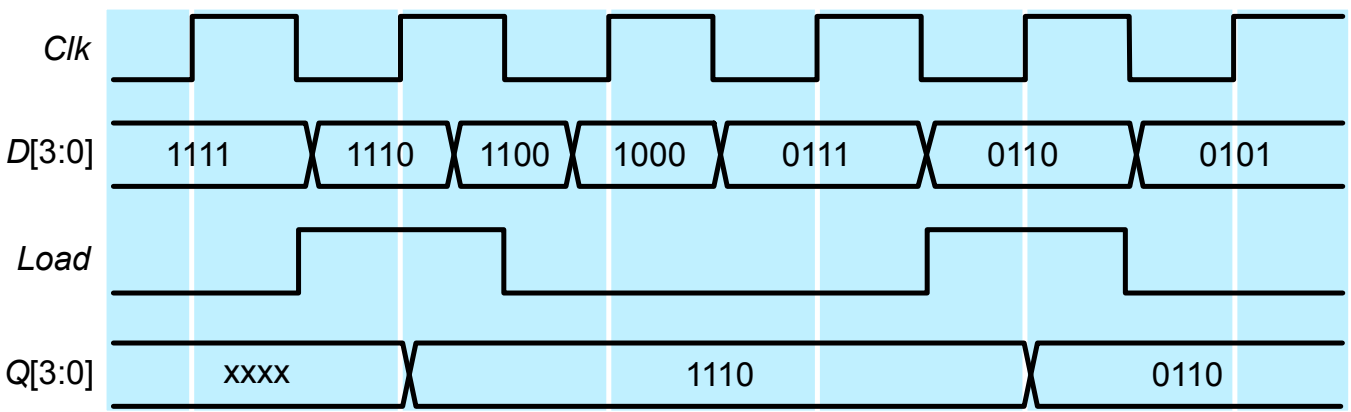
Resettable Register



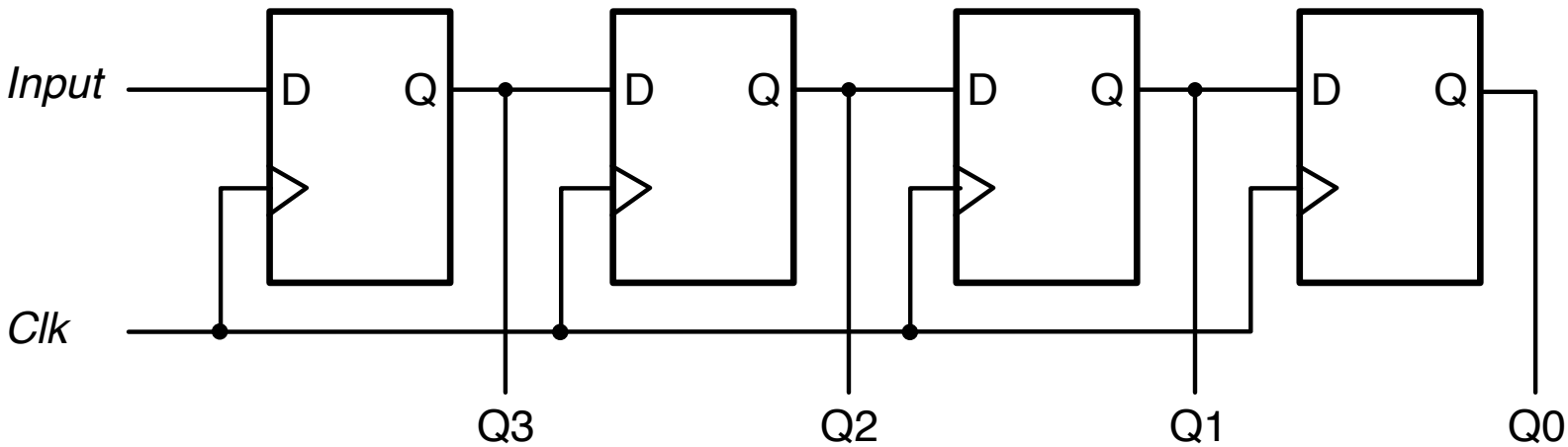


Register with Load Enable

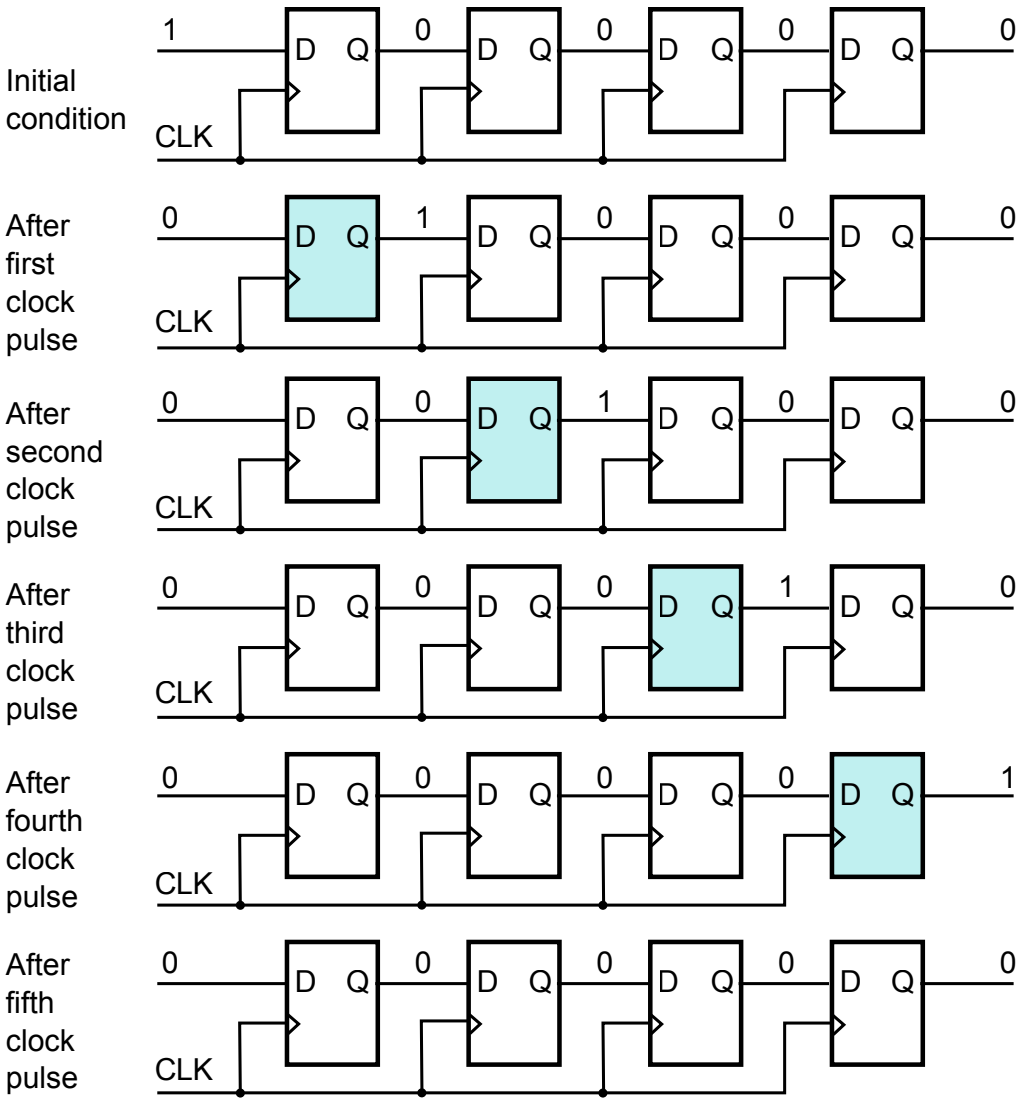




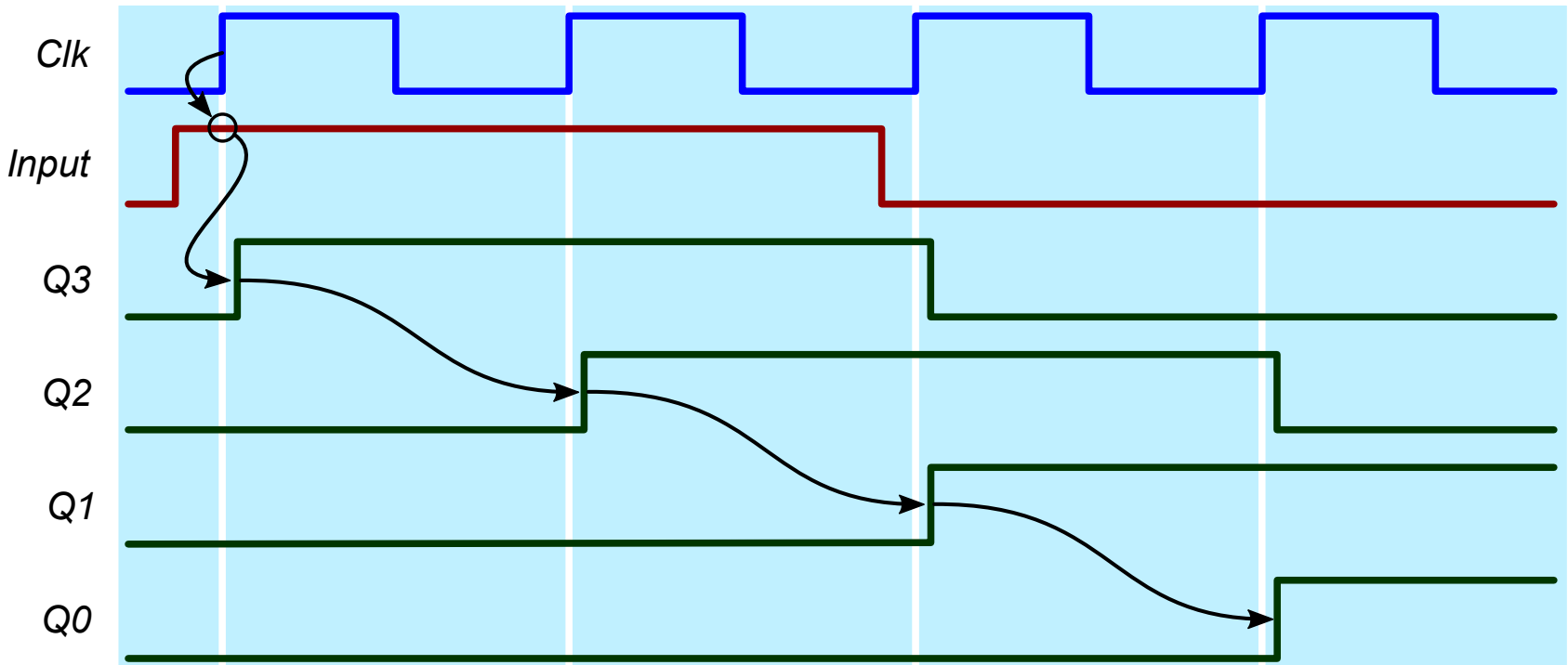
Basic Shift Register



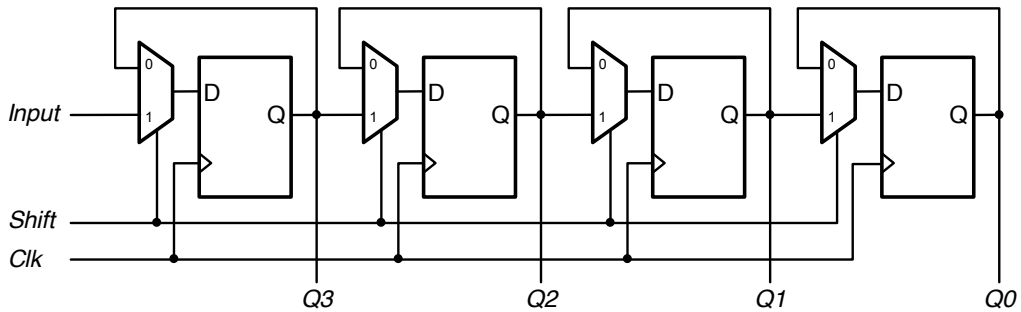
Shift Register “Animation”

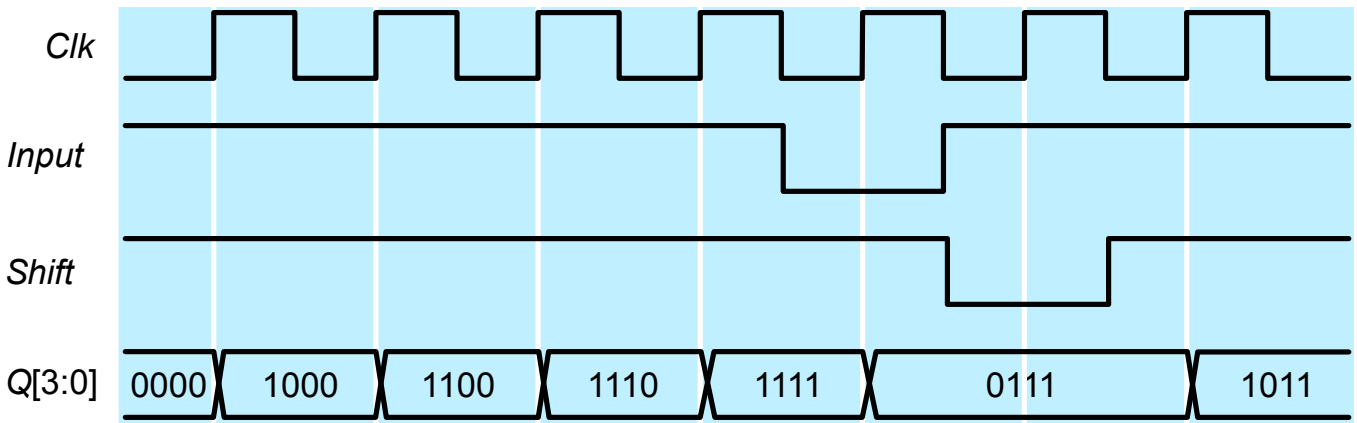


Shift Register Timing Diagram

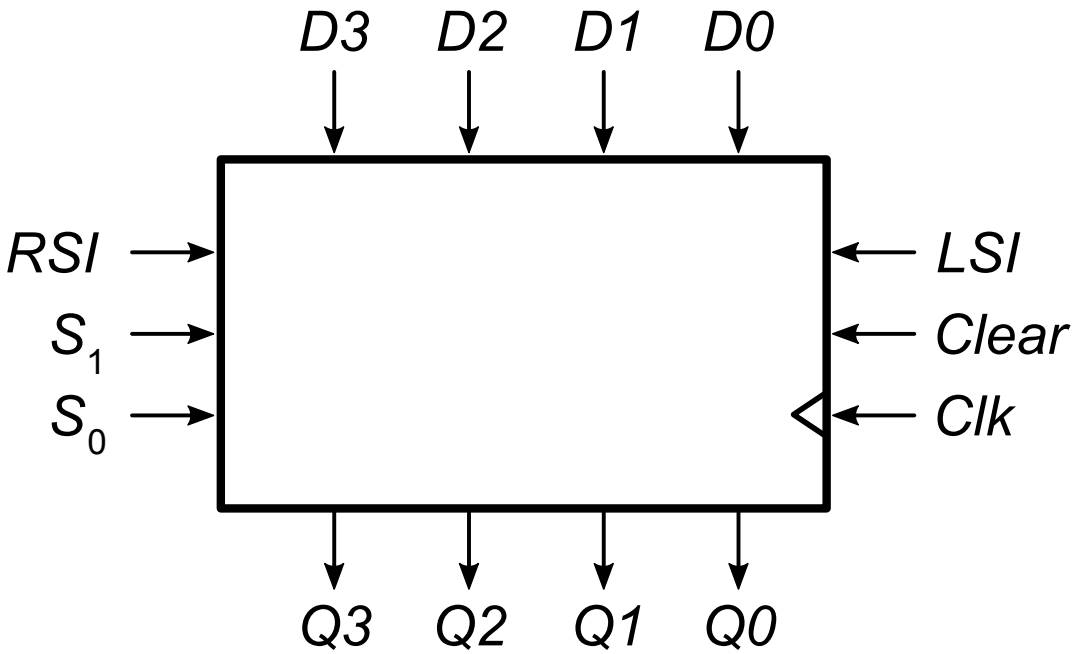


Enabled Shift Register





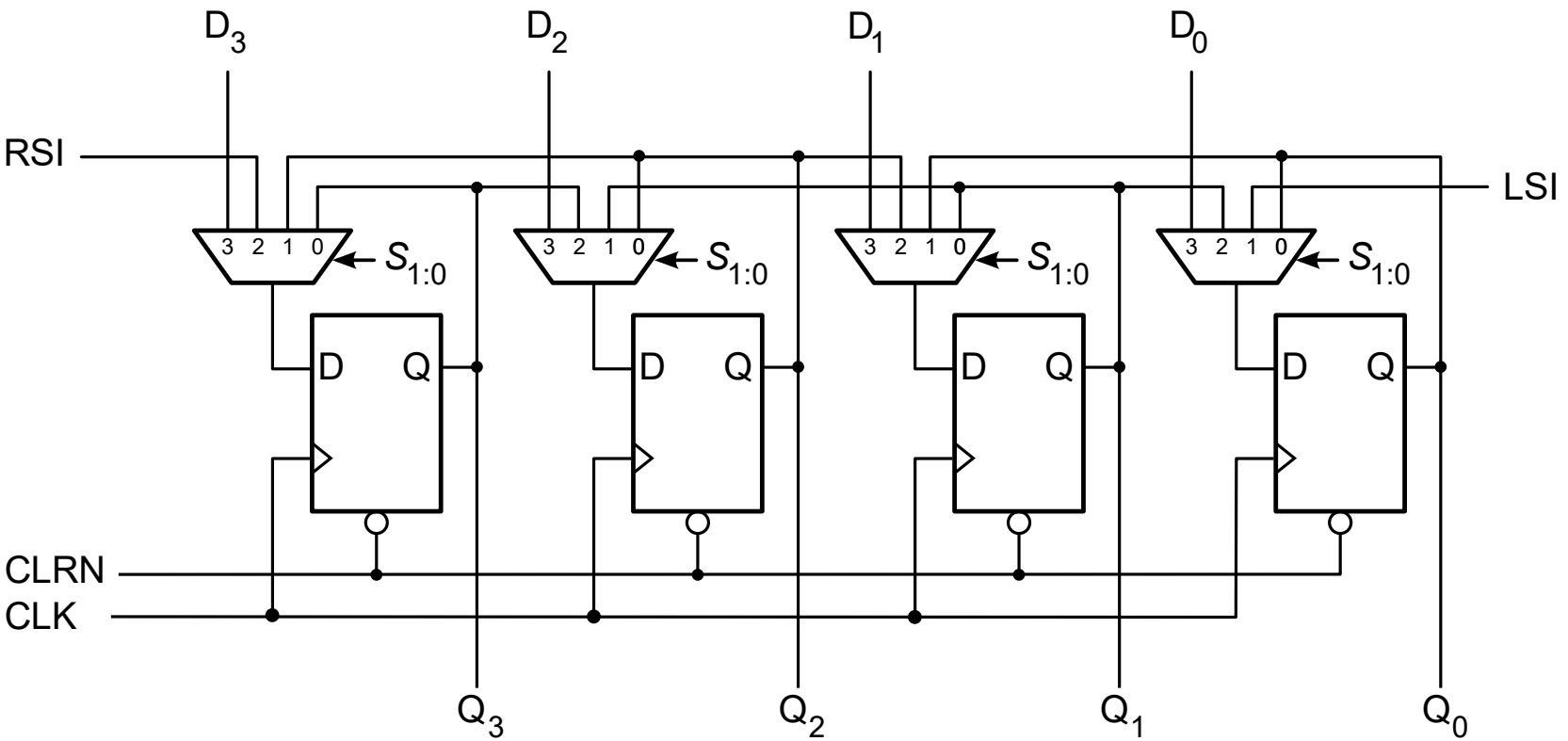
Universal Shift Register



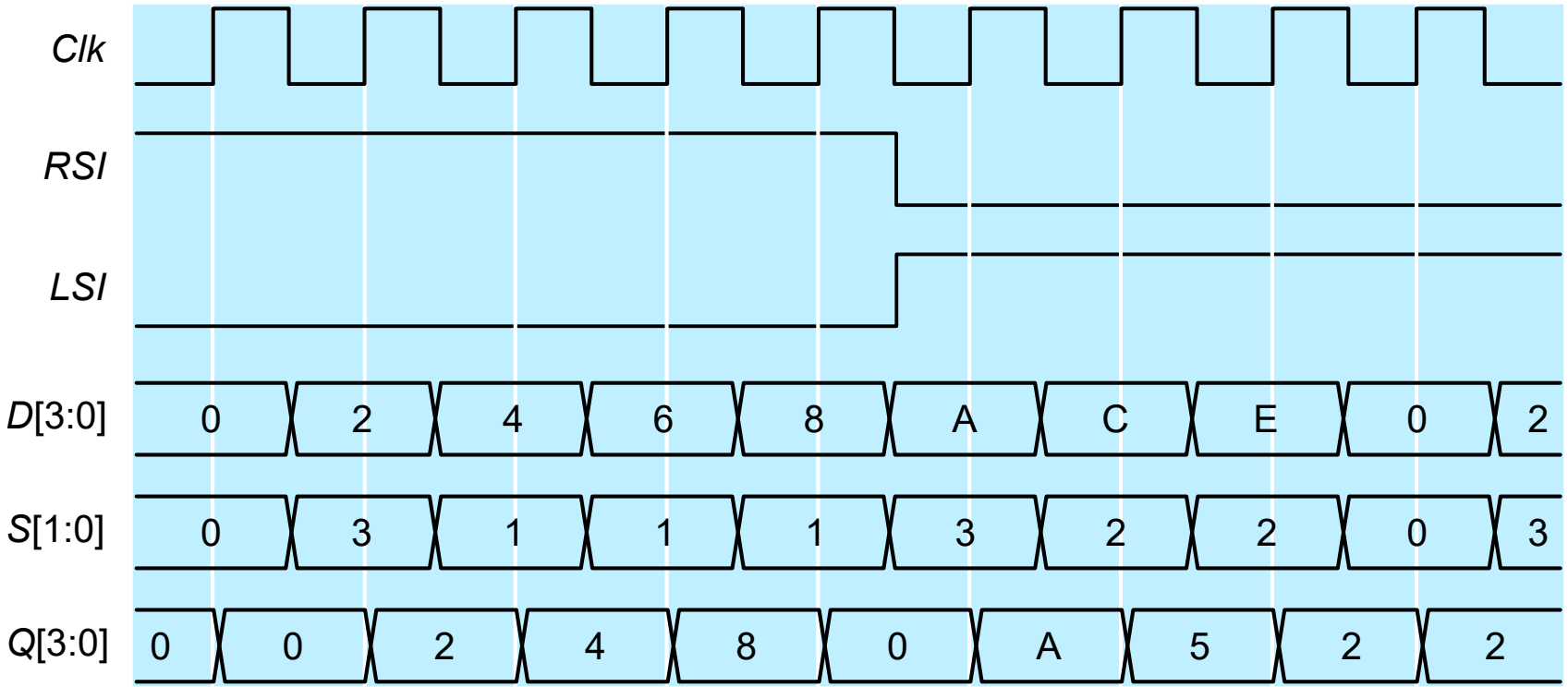
S_1	S_0	Function
0	0	Hold
0	1	Shift left
1	0	Shift right
1	1	Load new input

- Can be used in either serial-to-serial, serial-to-parallel, parallel-to-serial, parallel-to-parallel, left shifting as well as right shifting.
- Useful in arithmetic operations to shift data left for multiplication or to shift data right for division.

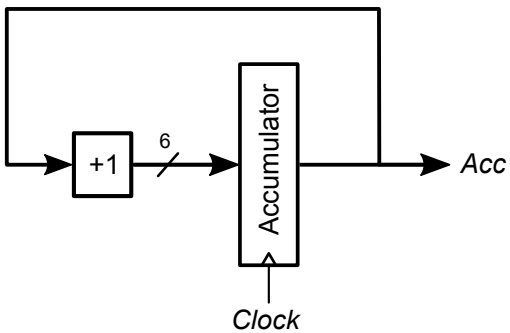
Universal Shift Register Schematic



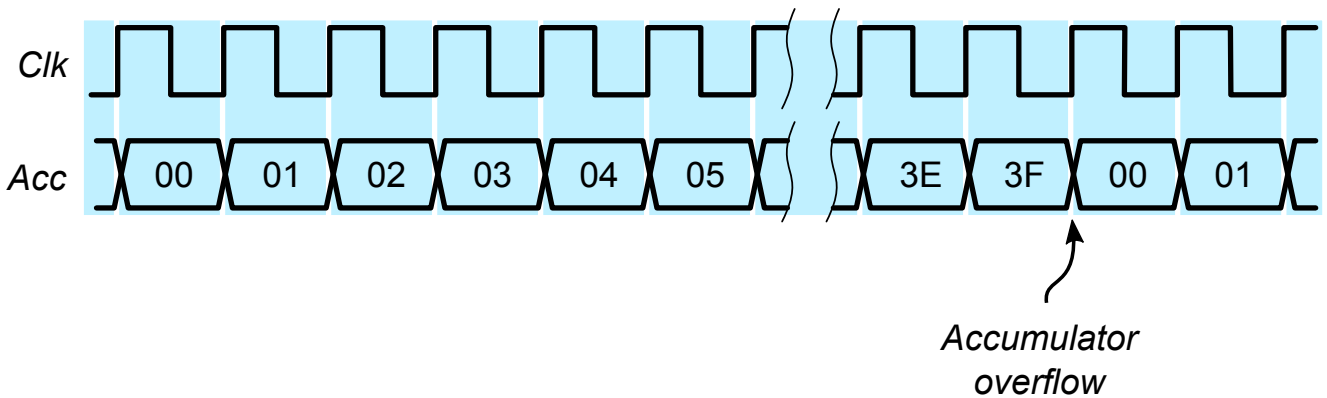
Universal Shift Register Timing Diagram



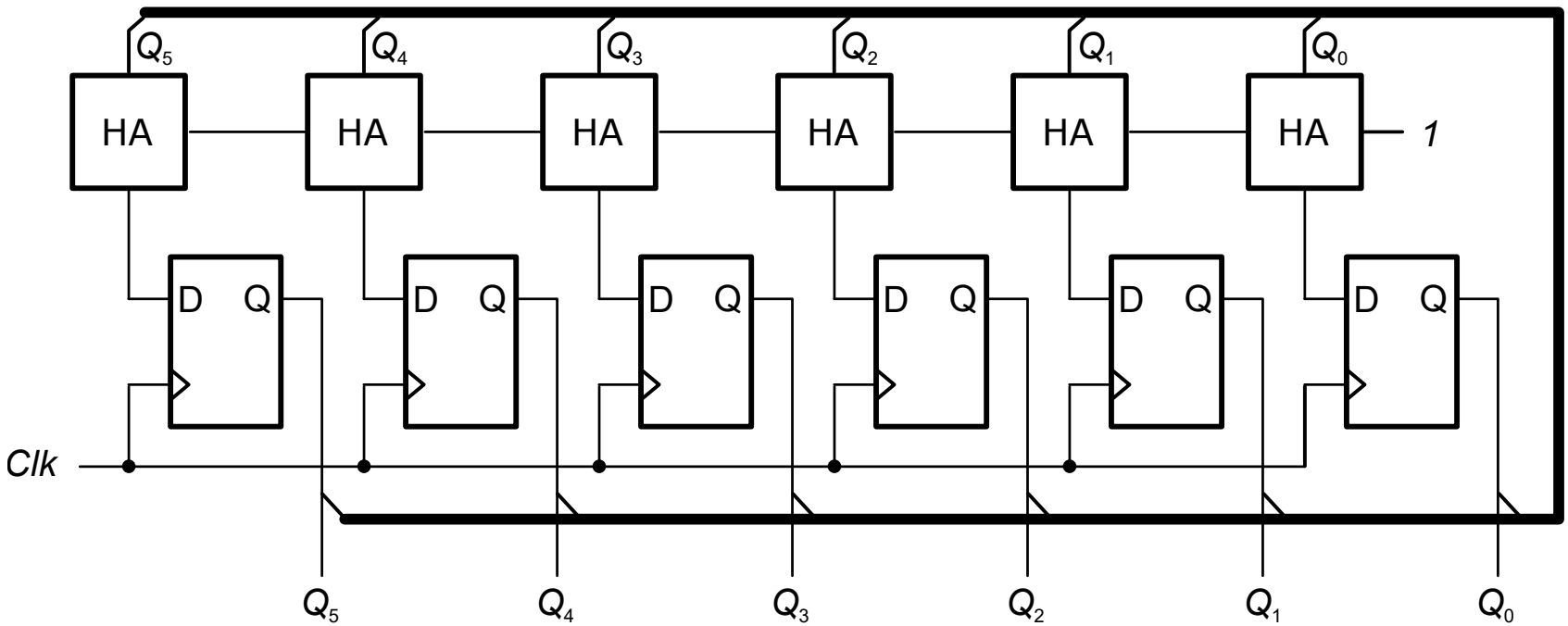
Accumulators



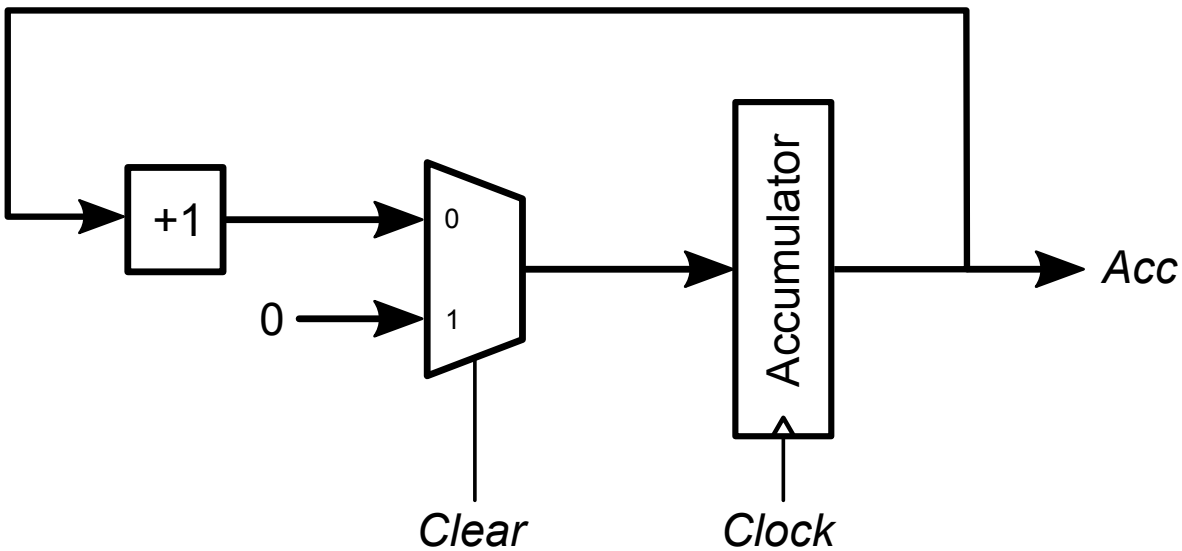
- Accumulator: register that keeps results of arithmetic ops.
- Registers + Adders $\rightarrow$ Accumulator-based counter.
- Any adder architecture may be used.



6-bit Accumulator-Based Counter



Resettable Counter

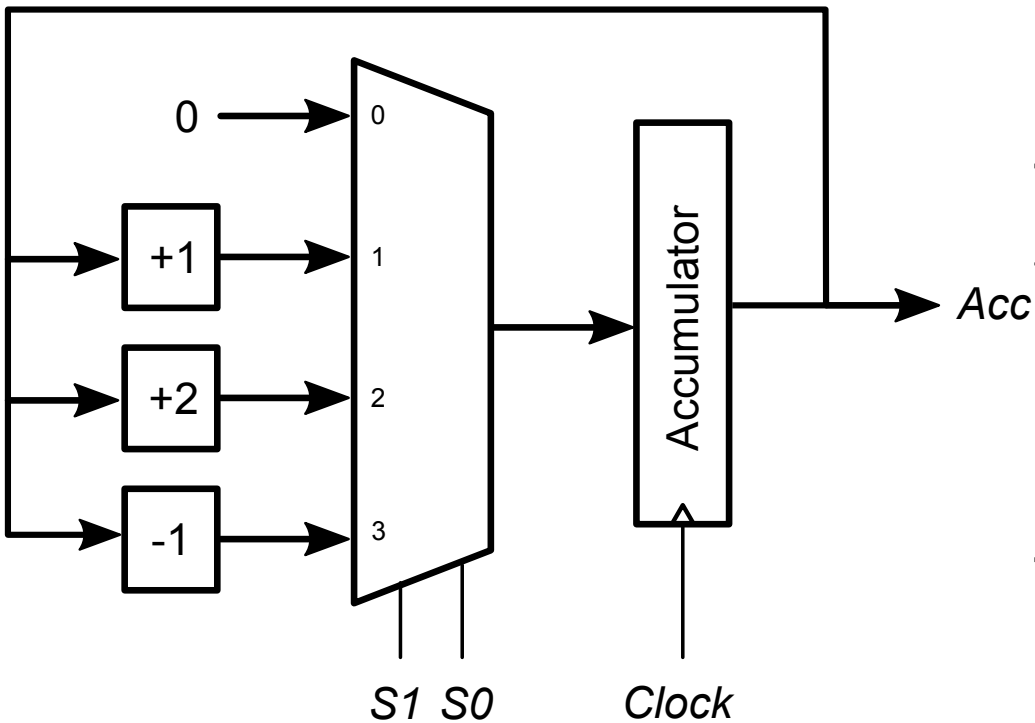


Clear	Function
0	Run
1	Clear

Check your understanding.

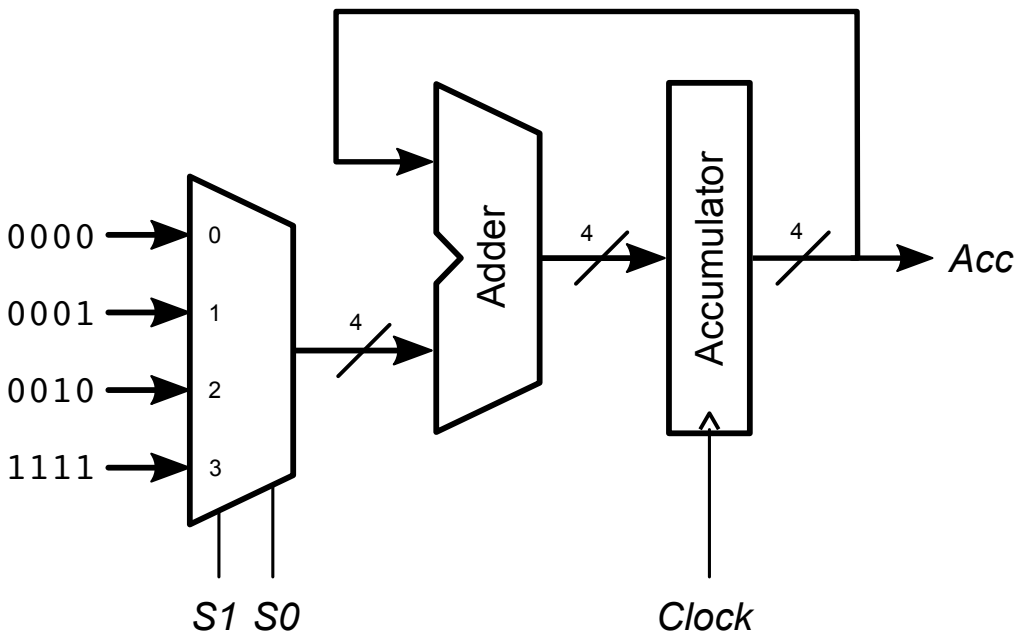
This is Milestone 2.

Multi-Function Counter No.1



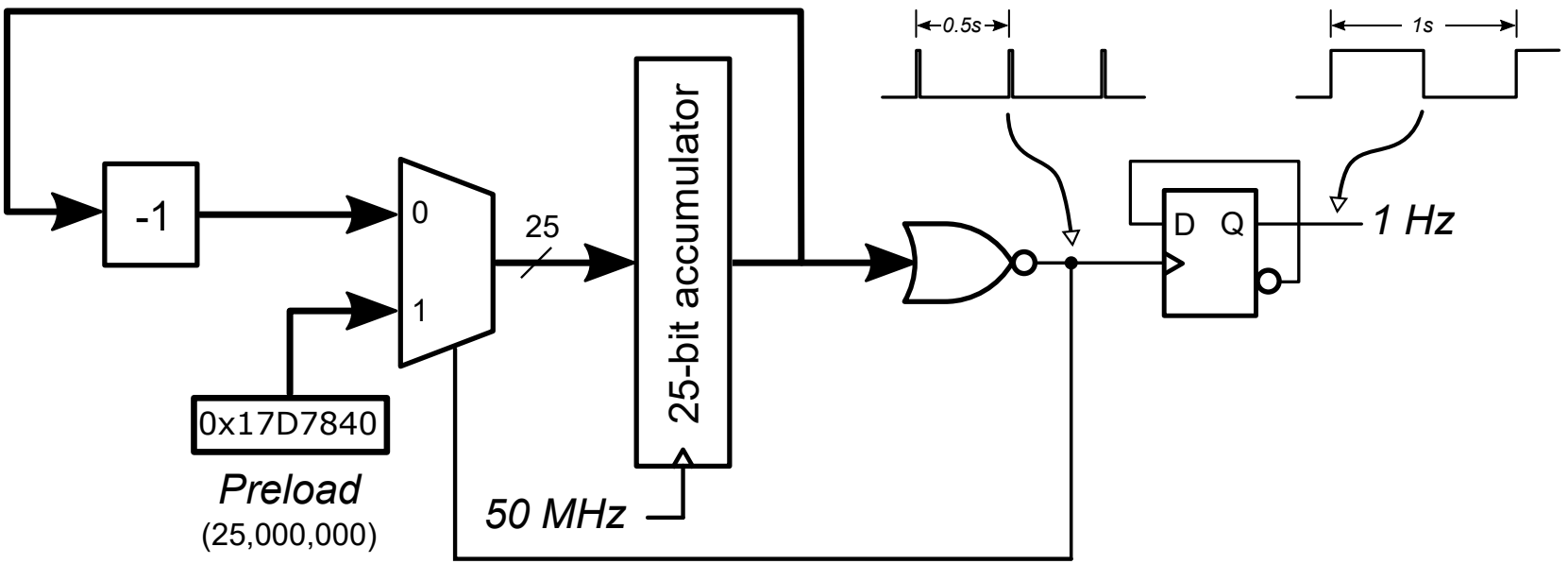
S1	S0	Function
0	0	Clear
0	1	Add 1
1	0	Add 2
1	1	Subtract 1

Multi-Function Counter No.2

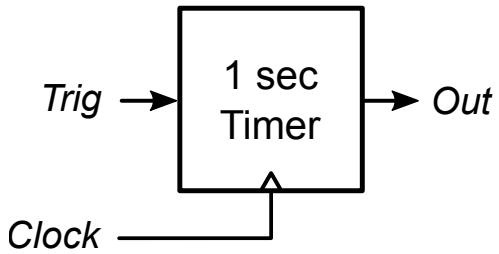


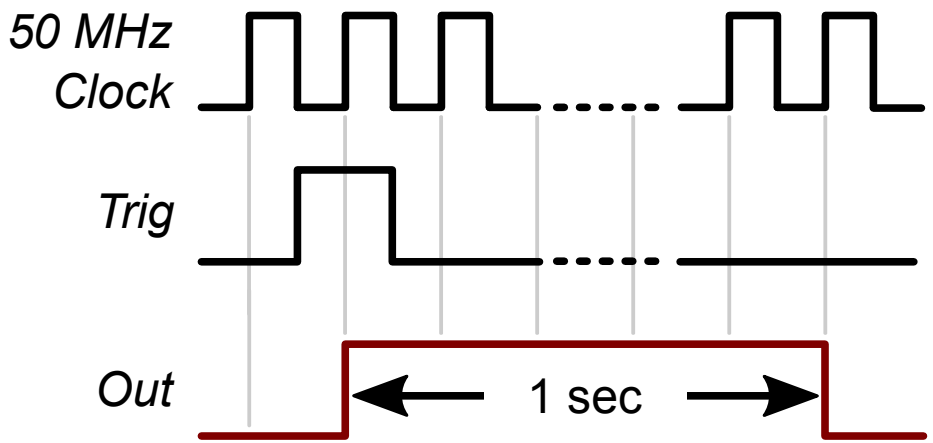
S1	S0	Function
0	0	Hold
0	1	Add 1
1	0	Add 2
1	1	Subtract 1

Prescaler

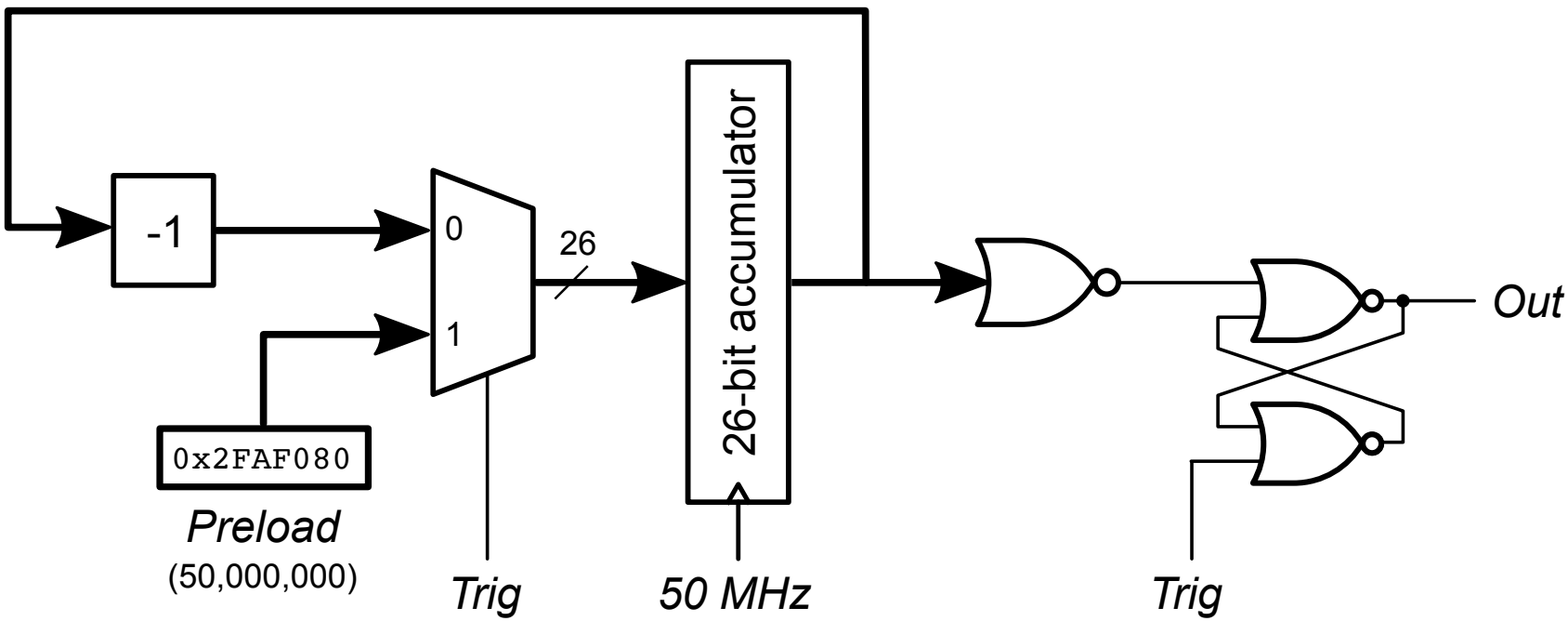

0.5s
1s
-1
0
1
25
25-bit accumulator
D Q
1 Hz
0x17D7840
Preload
(25,000,000)
50 MHz

Timer





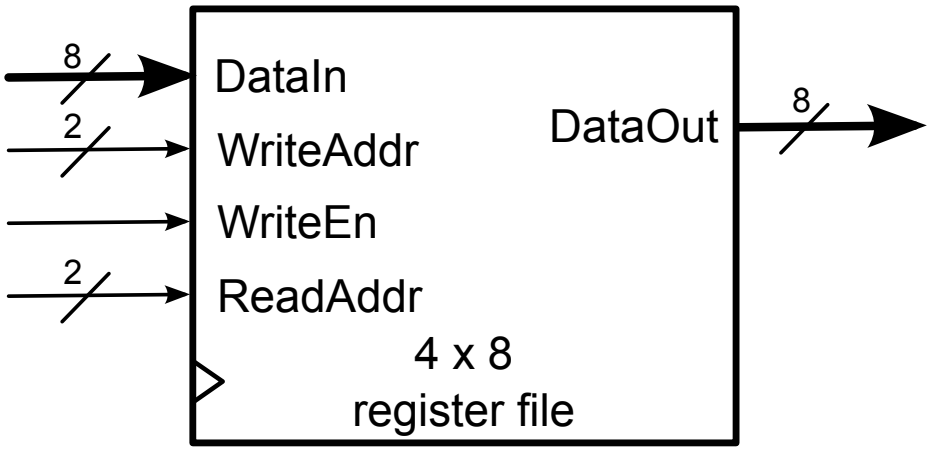
Timer


-1
0
1
26
26-bit accumulator
0x2FAF080
Preload
(50,000,000)
Trig
50 MHz
Trig
Out

Register Files vs RAM

	Register Files	**RAM**
Capacity	Small	Large
Speed	Fast	Slow
Ease of Design	Easy	Harder

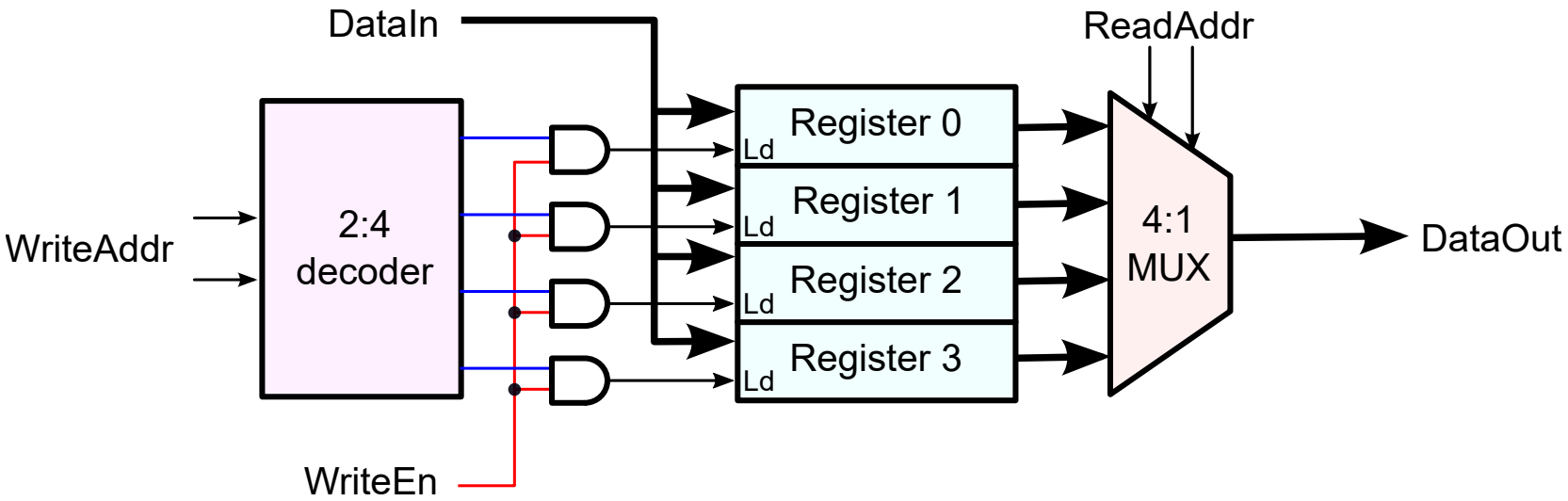
Minimal Register File



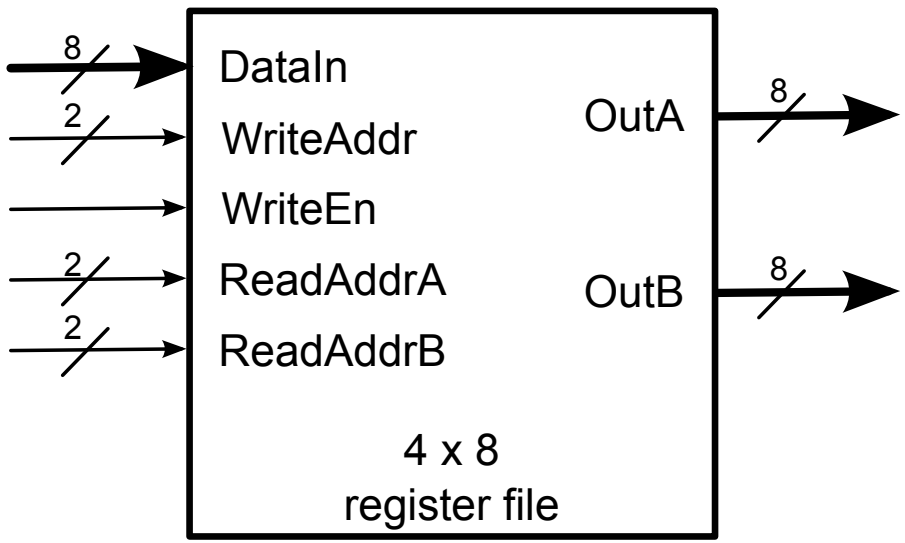
Four 8-bit registers

- DataIn : n-bit input
- DataOut : n-bit output
- WriteAddr: $log_2 n$-bit write address
- ReadAddr: $log_2 n$-bit read address
- WriteEn: write enable

Minimal Register File



Register File with 2 Read Ports



Register File with 2 Read Ports