

Chapter 7

Sequential Logic

SKEE2263 Digital Systems

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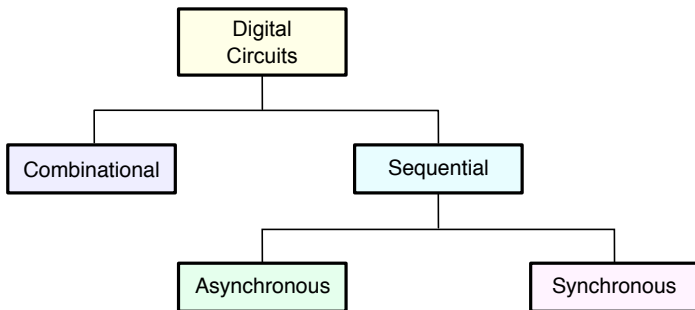
1 Intro

2 Bistable Circuits

3 FF Characteristics

4 FF Excitation

Classes of Digital Circuits

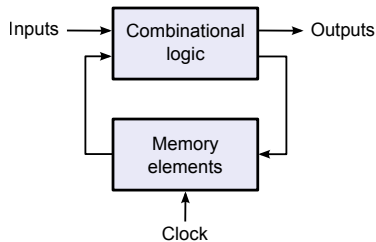
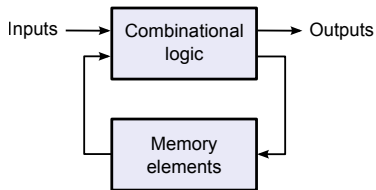


Sequential vs Combinational

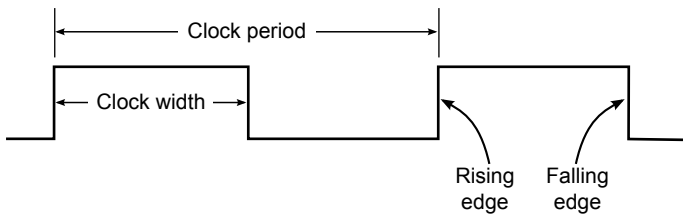
- Combinational:
 - Output = $f(\text{Present Input})$
 - Memoryless
- Sequential:
 - Output = $f(\text{Present Input, Past Input})$
 - Uses latches/flip-flop as memory
 - May have clock input (synchronous) or not (asynchronous)

Clocks

- Asynchronous sequential circuits have no clock input

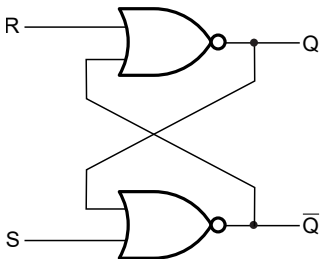


Clock Parts

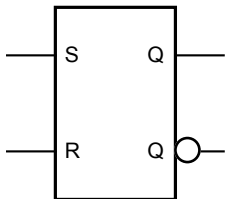


SR Latch: Gate Level

- Bistable circuits: stable in state 0 or 1
- Simplest bistable is SR latch

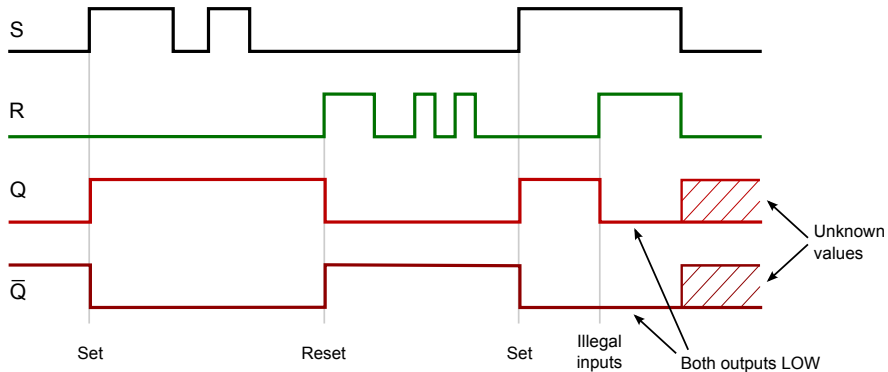


SR Latch: Logic Symbol, Characteristic Table

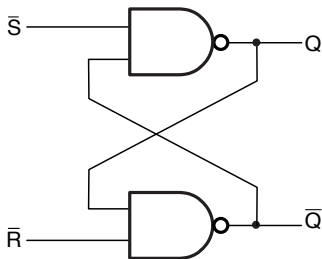


S	R	Q⁺	\bar{Q}^+	Action
0	0	Q	\bar{Q}	No change
0	1	0	1	Reset
1	0	1	0	Set
1	1	0	0	Forbidden

SR Latch: Timing Diagram

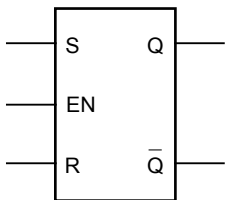


\bar{S} \bar{R} Latch: Gate Level, Characteristic Table



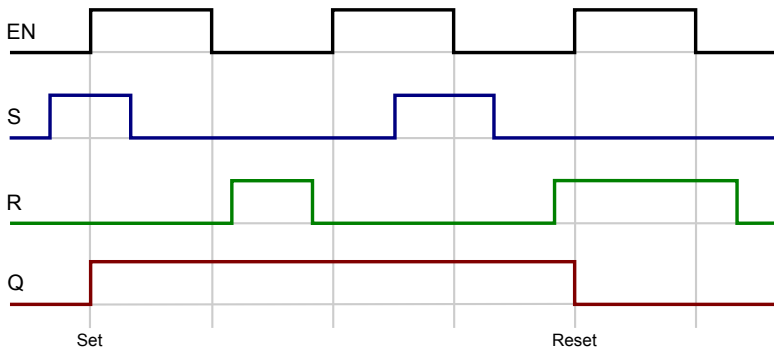
S	R	Q^+	\bar{Q}^+	Action
0	0	1	1	Forbidden
0	1	1	0	Set
1	0	0	1	Reset
1	1	Q	\bar{Q}	No change

Gated SR Latch: Logic Symbol, Characteristic Table

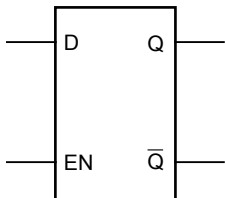


EN	S	R	Q ⁺	Action
0	×	×	Q	No change
1	0	0	Q	No change
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	×	Forbidden

Gated SR Latch: Timing Diagram

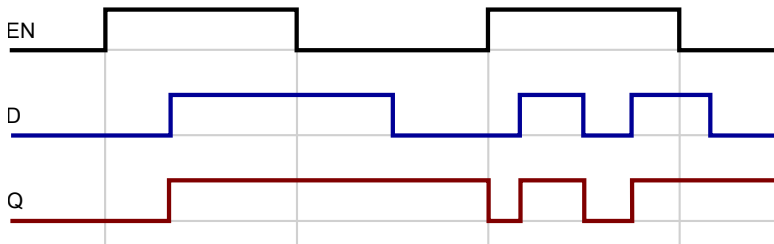


Gated D Latch: Logic Symbol, Characteristic Table

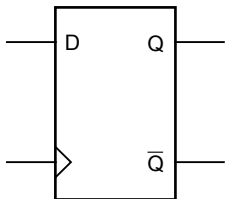


EN	D	Q⁺	Action
0	×	Q	Storage state
1	0	0	Transparent mode
1	1	1	Transparent mode

Gated D Latch: Timing Diagram

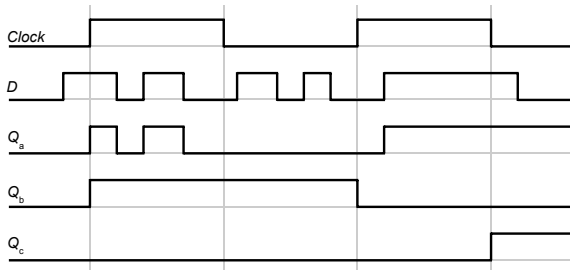
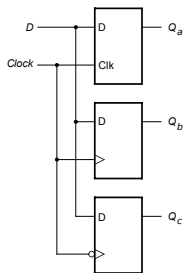


D Flip-Flop: Logic Symbol, Characteristic Table

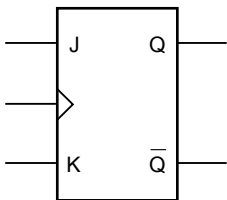


Clk	D	Q ⁺	Action
0	×	Q	No change
1	×	Q	No change
↑	0	0	Reset
↑	1	1	Set

D Flip-Flop vs Latch

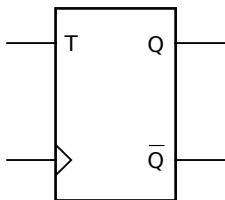


JK Flip-Flop: Logic Symbol, Characteristic Table



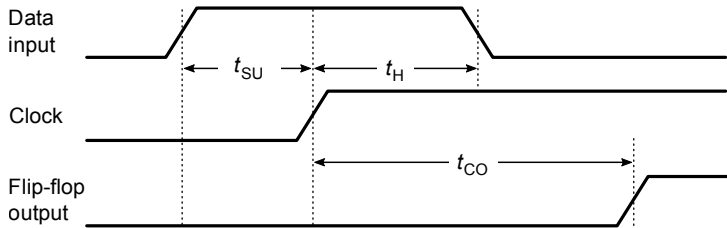
Clk	J	K	Q^+	Action
0	×	×	Q	No change
1	×	×	Q	No change
↑	0	0	Q	No change
↑	0	1	0	Reset
↑	1	0	1	Set
↑	1	1	Q'	Toggle

T Flip-Flop: Logic Symbol, Characteristic Table



Clk	T	Q^+	Action
0	x	Q	No change
1	x	Q	No change
↑	0	Q	No change
↑	1	Q'	Toggle

FF Timing Parameters



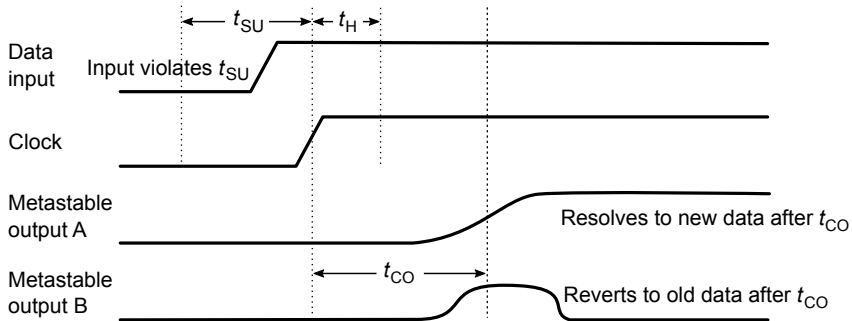
FF Timing Parameters

Setup time, t_{SU} – the minimum time that a flip-flop input must be stable before the clock edge.

Hold time, t_H – the minimum time after the clock edge that a flip-flop input must continue to be in the same stable state.

Clock to output delay time, t_{CO} – the minimum time after a clock edge to obtain a valid output

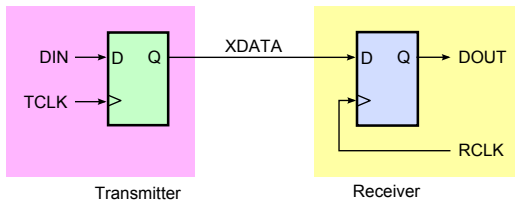
Setup Time Violation



Causes of Metastability

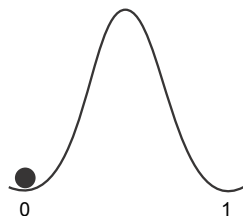


Asynchronous Inputs.

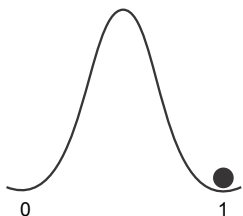


Data transfer across clock domains.

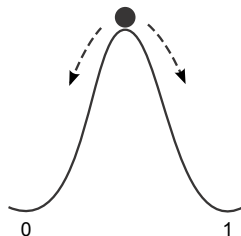
What Happens During Metastability



Stable state 0

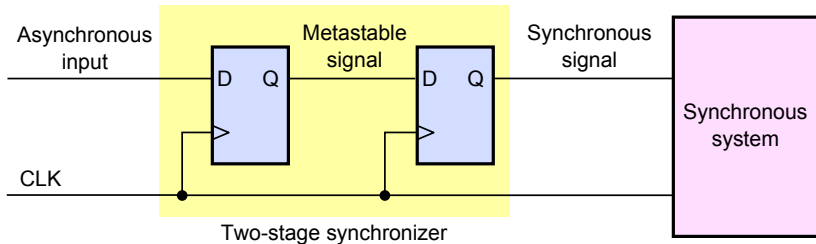


Stable state 1



Metastable state

Solution for Metastability



D Flip-Flop

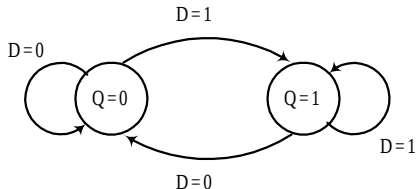
Characteristic table:

D	Q ⁺	Operation
0	0	Reset
1	1	Set

Excitation table:

Present State	Next State	Input
Q	Q ⁺	D
0	0	0
0	1	1
1	0	0
1	1	1

State diagram:



Characteristic Equation:

$$Q^+ = D$$

T Flip-Flop

Characteristic table:

T	Q ⁺	Operation
0	Q	No change
1	Q'	Complement

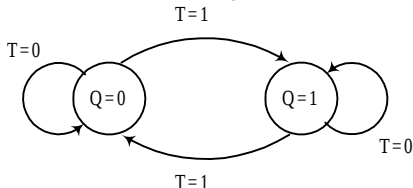
Excitation table:

Present State	Next State	Input
Q	Q ⁺	T
0	0	0
0	1	1
1	0	1
1	1	0

Characteristic Equation:

$$Q^+ = T'Q + TQ' = T \oplus Q$$

State diagram:



JK Flip-Flop

Characteristic table:

J	K	Q^+	Operation
0	0	Q	No change
0	1	0	Reset
1	0	1	Set
1	1	Q'	Complement

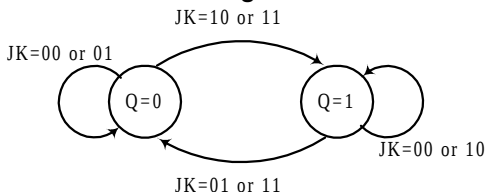
Excitation table:

Present State Q	Next State Q^+	Inputs	
		J	K
0	0	0	×
0	1	1	×
1	0	×	1
1	1	×	0

Characteristic Equation:

$$Q^+ = J\bar{Q} + \bar{K}Q$$

State diagram:



SR Flip-Flop

Characteristic table:

S	R	Q^+	Operation
0	0	Q	No change
0	1	0	Reset
1	0	1	Set
1	1	?	Undefined

Excitation table:

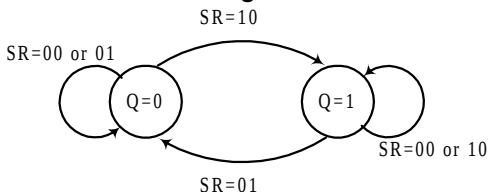
Present State	Next State	Inputs	
Q	Q^+	S	R
0	0	0	×
0	1	1	0
1	0	0	1
1	1	×	0

Characteristic Equation:

$$Q^+ = S + \bar{R}Q$$

$$SR \neq 1$$

State diagram:



Excitation Table Summary

Q	Q⁺	S	R	D	J	K	T
0	0	0	×	0	0	×	0
0	1	1	0	1	1	×	1
1	0	0	1	0	×	1	1
1	1	×	0	1	×	0	0