SKEE2263
Milestone 1
Individual
(5% final grade)

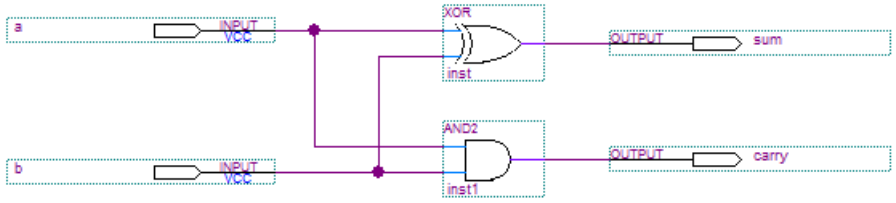
Objectives:

- Familiarization with Altera Quartus for entering, compiling and simulating a logic design.
- Describing a complex digital system using hierarchy, modularity and regularity
- Using the Internet to find solutions of circuit designs.

Part 1A: Half adder

Step 1.

Enter schematic diagram of a half adder.



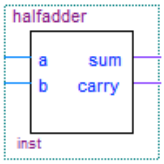


Fig 1.

a	b	carry	sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Step 2.

Compile the design.

Step 3.

Simulate by giving all 4 input combinations for a and b. If there are no errors, print the simulation report.

Step 4.

Print the following pages as PDF. It is preferred that you choose landscape format.

Page 1: Circuit schematic
Page 2: Simulation output waveform. *This is not the same as the simulation input.*

Part 1B: Full adder

Step 1.

Enter the Verilog for implementing a full adder using the half adder module from Part 1A and one OR gate. Your design must contain exactly the three components shown below. A design implemented using just gates does not comply with the concept of hierarchy and modularity.

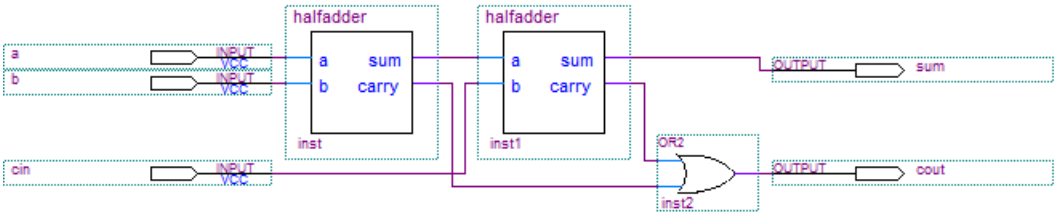


Fig 2.

Steps 2.

Compile until there are no errors.

Step 3:

Simulate using all 8 input combinations. The inputs and outputs must match the full adder truth table before going to Step 4.

Step 4.

Print the following pages as PDF, preferably in landscape format.
Page 3: Circuit schematic
Page 4: Simulation report. *Do not give the input waveform*.

Part 1C: Ripple adder

Step 1.

Enter the schematic for a 4-bit parallel adder as shown in Fig. 3. You must use only full adder blocks.

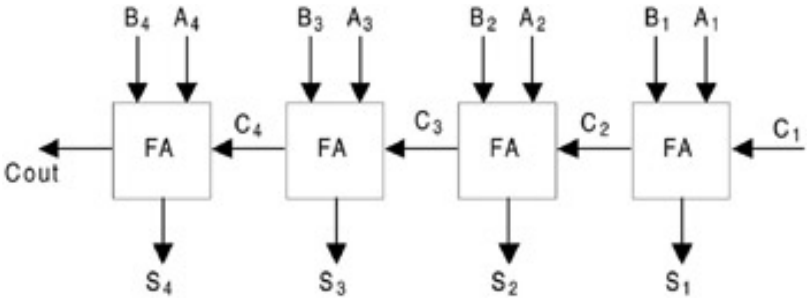


Fig 3.

Steps 2.

Compile until there are no errors.

Steps 3.

Complete the table so you know what to expect.
Simulate using only the given test data. Use grouping in the waveform to simplify your work.
Then mark in the table whether your adder complies with expected results.

Table 1C					
$A_3a_2a_1a_0$	$b_3b_2b_1b_0$	c_{in}	c_{out}	$s_3s_2s_1s_0$	Comply?
0000	0000	0			
0000	0000	1			
1111	1111	0			
1111	1111	1			
1111	0101	0			
0000	1010	1			
0011	1100	0			
0101	1010	1			

Step 4.

Print the following pages as PDF.

Page 5: Ripple adder schematic
Page 6: Simulation output waveform and completed Table 1C.
Page 7: At least 3 references. On this page, list all web sites, articles or books you referred in completing the assignment. You must any citation format but be consistent. For example, you can use the APA style found here:
https://www.library.cornell.edu/research/citation/apa

Step 5.

Combine all 7 PDF pages into 1 PDF document. Add a front cover. Submit.