

**SKEE2263  
Term Project  
Student Guide**

Beginning this semester, 30% of your final marks are derived from the term project. At the end of term, you must implement a complete digital system on an Altera FPGA board. The titles available for the project are listed on a separate document. To ensure you successfully complete the project, the term project has 6 different tasks, so that you build the complete system incrementally. The following Gantt Chart outlines the tasks.

#	Task	Week														
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	Quartus familiarization	█	█													
2	Altera built-in module familiarization			█	█											
3	Construction of combinational modules					█	█	█								
4	Construction of sequential modules								█	█	█					
5	Datapath unit integration											█	█			
6	Control unit implementation													█	█	█

The end of each task is a milestone, and you are to deliver the following:

Milestone	Date	Deliverable
1	Early week 3	Multi-bit adder
2	Early week 5	4-bit to 7-segment decoder
3	Before break	Combinational modules of your chosen circuit
4	Early week 11	Sequential modules of your chosen circuit
5	Early week 13	Datapath unit combining all previously designed modules
6	During week 15	Completed system combining datapath unit and control unit

Completion of a milestone is worth 5% of the overall grade.

Task 1 & 2 are common. Everybody is to complete them individually. Involves simulation only.

Tasks 3-6 are done in groups of 3.